(5)

DEFENSE ADVANCED RESEARCH PROJECTS AGENCY

MICROWAVE AND MILLIMETER WAVE MONOLITHIC
INTEGRATED CIRCUITS (MIMIC) PROGRAM

MIMIC BRIEFS

Summaries of Phase 3 Technology Support Programs

JANUARY 1993

Prepared by:
PALISADES INSTITUTE FOR RESEARCH SERVICES, INC.

REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION Unclassified, No Foreign Nationals	1b. RESTRICTIVE MARKINGS
2a. SECURITY CLASSIFICATION AUTHORITY ----------	3. DISTRIBUTION / AVAILABILITY OF REPORT Approved for distribution to all qualified DTIC users.
2b. DECLASSIFICATION / DOWNGRADING SCHEDULE ----------	
4. PERFORMING ORGANIZATION REPORT NUMBER(S) ----------	5. MONITORING ORGANIZATION REPORT NUMBER(S)
6a. NAME OF PERFORMING ORGANIZATION Palisades Institute for Research Services, Inc. 6b. OFFICE SYMBOL (If applicable) -------	7a. NAME OF MONITORING ORGANIZATION Defense Advanced Research Projects Agency (DARPA)
6c. ADDRESS (City, State, and ZIP Code) 2011 Crystal Drive Arlington, VA 22202	7b. ADDRESS (City, State, and ZIP Code) 3701 N. Fairfax Dr. Arlington, VA 22203-1714
8a. NAME OF FUNDING / SPONSORING ORGANIZATION DARPA/ESTO 8b. OFFICE SYMBOL (If applicable)	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER MDA972-89-C-0087 SPC-PIRS-90-C-15
8c. ADDRESS (City, State, and ZIP Code)	10. SOURCE OF FUNDING NUMBERS PROGRAM ELEMENT NO.: PE0603706E PROJECT NO.: TASK NO.: WORK UNIT ACCESSION NO.:

11. TITLE (Include Security Classification)

MIMIC Briefs: Summaries of Phase 3 Technology Support Programs (U)

12. PERSONAL AUTHOR(S)
Kramer, Warner (703) 486-7103

13a. TYPE OF REPORT	13b. TIME COVERED	14. DATE OF REPORT (Year, Month, Day)	15. PAGE COUNT
Project Summaries	FROM Jul. 90 TO Dec 92	January 1993	58

16. SUPPLEMENTARY NOTATION

17. COSATI CODES			18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB-GROUP	Monolithic Microwave Devices, Microwave Integrated Circuits, MIMIC, MMIC, Millimeter Wave Devices, Gallium Arsenide (GaAs), MESFET, Analog Microcircuits, MHDL, On-Wafer

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

This publication contains technical and contractual summaries of the MIMIC program's Phase 3 technology support programs. Each project description includes a discussion of the objectives of the effort, the approach pursued and recent progress. Also identified are the performing organization(s), principal investigator and/or other key personnel, contract number, program funding and duration, and program monitor/COTR. Concluding the document is a directory of the personnel associated with these projects, from whom more information may be requested.

20. DISTRIBUTION / AVAILABILITY OF ABSTRACT	21. ABSTRACT SECURITY CLASSIFICATION
☒ UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT. ☐ DTIC USERS	Unclassified

22a. NAME OF RESPONSIBLE INDIVIDUAL	22b. TELEPHONE (Include Area Code)	22c. OFFICE SYMBOL
Elissa Sobolewski	(703) 696-2254	DARPA/ESTO

Block Number 18 (con'd)

Testing, Improved GaAs Growth Techniques, Multi-chip Pakcages, Molecular Beam Epitaxy (MBE), MOCVD, Focused Ion Beam (FIB).

PREFACE

This document presents an updated summary of the Phase 3 portion of the DARPA-sponsored Microwave and Millimeter Wave Monolithic Integrated Circuits (MIMIC) program. The Phase 3 programs are highly focused technology support efforts whose aim is to help ensure the ultimate success of the MIMIC program. The primary goal of the MIMIC program is to provide affordable, reliable products for DoD systems on a continuing basis.

There have been 26 MIMIC Phase 3 contracts awarded since 1989, addressing such critical areas as gallium arsenide (GaAs) wafer characterization, improved GaAs growth techniques, MIMIC modeling and computer aided design (including MHDL), on-wafer testing, packaging technology, advanced processing techniques, and foundry fabrication of specific MIMIC chips. All 26 contracts, both active and completed, are discussed in this report.

The format of this second edition of the MIMIC Briefs has not changed. As before, each program description includes a discussion of the objectives of the effort, the approach pursued and recent progress. Also indicated are the performing organization(s), principal investigator(s), contract number, program funding and duration, and government program monitor(s). A summary chart on pages 48-49 presents a record of MIMIC Phase 3 funding through Phase 3 program completion.

More information may be requested from the personnel associated with each program. A personnel directory appears on pages 51-58.

TABLE OF CONTENTS

1. MATERIALS AND IMPROVED GALLIUM ARSENIDE (GaAs) GROWTH TECHNIQUES

1.1 Optical Diagnostics for Wafer Characterization

PERF. ORGS.:	AT&T Bell Labs; Hughes-MPD
KEY PERSONNEL:	Vince Zaleckas (AT&T), Hilda Kanber (Hughes), Gary Carver (AT&T), Greg Koos (AT&T)
CONTRACT NO.:	F33615-89-C-1054
FUNDING:	$566,041
PERIOD:	7/89-12/91
COTR:	Capt. Dennis May

OBJECTIVES/APPROACH: The objective of this program was to develop a capability for nondestructive optical characterization of defects and impurities in GaAs wafers. Wafers were characterized using optical diagnostic techniques; complementary conventional characterization was used for comparison, and microwave devices with test structures were fabricated for yield correlation studies. The ultimate goal was to develop diagnostic techniques capable of screening low quality material prior to device processing.

AT&T Bell Laboratories, Princeton, NJ, was responsible for developing the optical diagnostic techniques used for wafer screening. Hughes-MPD, Torrance, CA, was responsible for providing appropriate wafers, performing conventional characterization, and conducting the device fabrication and yield correlation studies.

The specific optical techniques developed under the program were OBIR (Optical-Beam Induced Reflectance), SRPL (Spatially Resolved Photoluminescence) and DLIM (Differential Laser Impurity Monitor). The OBIR system allows for the nondestructive spatial mapping of electrically active defects near the surface of semiconductor wafers. The system functions by pumping the surface with a focused argon laser beam, and then probing the resulting photo-induced change in the reflectance of a CO_2 laser. This combines the advantages of highly focused visible light with the sensitivity to carrier density exhibited by infrared radiation. As the beams are scanned over a wafer, strong IR modulation is indicative of good material while weak IR modulation reveals the presence of electrically active defects. The measurement is tuned to the surface, has a spatial resolution of 1 μm and operates at room temperature in air. SRPL was incorporated into the OBIR system via the addition of appropriate optics and detectors. DLIM relies on making a fast comparison of the transmittance between a standard GaAs wafer with a known impurity concentration and a wafer of unknown concentration. Differences in wafer thickness and background doping between the two wafers can be accounted for. Signal-to-noise ratios can be improved by two orders of magnitude over that of FTIR (Fourier Transform Infrared) through the use of lead salt lasers because nearly all of the generated power can be tuned within the linewidth of local vibrational modes associated with the impurity of interest.

The program was divided into seven major tasks:

Task 1: Material characterization and yield correlations. In addition to MIMIC Phase 1 insertion, a major milestone for the Phase 3 program occurred here, the correlation of OBIR/SRPL and DLIM data to device yield.

Tasks 2, 3 and 4: Specific development of OBIR/SRPL diagnostic capability, initially at 30 s frame rates followed by video rates. Milestones included correlation of OBIR/SRPL operation at high throughput (video) rates.

Task 5, 6 and 7: Specific development of DLIM for detection of impurities, including carbon, boron and silicon. The final task was to be a demonstration of wafer mapping under computer control.

PROGRESS (Source: D. May, 4/92 and V. Zaleckas, 9/92): This program has largely achieved its technical objectives with some cost growth and some delay. The final report details the following:

Task 1: Good correlation was achieved between electrically active defects observed on unprocessed wafers and device performance anomalies seen on these same wafers after processing. The scanning process is still believed to cause no damage. AT&T has contacted another party to have the system manufactured for sale to other users.

Tasks 2, 3 and 4: Video rate scanning has been achieved. Correlation information has been developed.

Tasks 5,6 and 7: These tasks have been completed but sensitivity is still deficient due to the quality of available lasers and mechanical vibration problems.

Although optically evaluated reticles were unable to reveal lineage boundaries, it is felt that subsequent work within Phase 2, carried on in collaboration with AT&T's Reading-PA group, will succeed in getting these SRPL maps to reveal those features. Ongoing work with Reading will evaluate the device impact of the lineage. A collaboration with Reading and Wright State University is comparing SRPL maps with PBS (photon backscatter) and EL2 (electroluminescence) maps. Potential future work with Hughes would apply SRPL maps to epitaxial structures.

The final technical report has been completed. Copies should soon be available through the Defense Technical Information Center (DTIC).

1.2 Cost Reduction and Quality Improvement in Epitaxial Materials for MMIC Applications

PERF. ORG.:	Bandgap Technology Corp.
KEY PERSONNEL:	Thomas J. O'Neill
CONTRACT NO.:	N00019-92-C-0111
FUNDING:	$839,000
PERIOD:	9/92-4/94
COTR:	Gerald M. Borsuk

OBJECTIVES/APPROACH: The objective of this project is to develop MBE material growth technology and to identify materials issues limiting wafer quality. The effort will address the issue of wafer cost reduction for 3- and 4-inch MBE HEMTs; seek improvement of wafer quality,

uniformity and reproducibility; and demonstrate this improvement through a detailed material-device correlation with MIMIC Phase 2 foundries.

Specifically, the aim is to develop nondestructive characterization methods, reduce destructive testing, improve growth reactor control, lower defect density, tighten control of the fabrication process, and obtain higher yield. Scanning photoluminescence and photoreflectance characterization of pHEMT wafers will be carried out and correlated with destructive tests such as SIMS and STEM. Critical data relating to AlGaAs and InGaAs alloy composition and thickness and the perfection and uniformity of the AlGaAs/InGaAs channel interface will be analyzed. A database will be established to correlate processed pHEMT device results with wafer material characterization.

Eleven lots of six wafers each will be processed for pHEMT test structures at Bandgap. Both 3- and 4-inch pHEMT wafers will be employed on this program. Each lot will be comprised of test wafers which explore the reproducibility and automation of multiple-wafer MBE growth, the development of nondestructive techniques such as photoreflectance and photoluminescence, etc. For instance, comparative studies of "identical" pHEMT structures made by single-wafer and multiple-wafer MBE systems wherein different nondestructive photoreflectance spectra are obtained are currently being made at Bandgap.

Bandgap's test structure findings will be confirmed by three complete continuous process improvement cycles which will include inputs from pHEMT MMIC manufacturing at Hughes MPD and Raytheon MMC. Raytheon will use a pHEMT structure designed for power applications, while Hughes will employ a structure supporting low noise applications. Both 3- and 4-inch wafers will be supplied to these foundries. Using their standard MIMIC Program pHEMT processing, the two foundries will fabricate both test structures and MMIC test vehicles. On-wafer dc and RF testing will be performed, and correlations between MMIC yield/performance, test structure data, materials quality assurance testing, and MBE growth procedures will be generated.

In 1991, the cost of pHEMT epitaxial structures was \$39.47/cm^2. By 1994, it is hoped to cut that cost to \$17.81/cm^2 for low-volume, 3-inch manufacturing, and to \$14.64/cm^2 for high-volume, 4-inch manufacturing.

PROGRESS (Source: H. B. Dietrich, 1/93): D. S. Katzer and H. B. Dietrich of NRL made a recent visit to Bandgap and found the program to be on track. During this visit, the Bandgap investigators presented work recently done to establish the correlation between the pHEMT structure and the variety of photoluminescence (PL) and photoreflectance (PR) signatures they have observed. This is a major step forward in the attempt to establish nondestructive methods for the characterization of the pHEMT material.

PHEMT structures with various growth treatments and buffer layer configurations were grown by MBE. The active layers of these pHEMT structures conformed to the Raytheon specifications. Down-time of Bandgap's MBE reactors due to system breakage, source reloading and the installation of a second multi-wafer reactor was relieved during November. This allows rapid schedule recovery for the growth of additional pHEMT structures for the program, and for the subsequent processing and test of these wafers.

The interface contamination/buffer reduction wafers were examined using standard quality assurance measures and nondestructive PL and PR methods. Differences in substrate preparation

procedures, buffer layer thicknesses, and superlattice buffer positions were evident with PL and PR testing.

Activities for pHEMT material-device correlation are confined to the establishment of database linkages between Bandgap, Raytheon, Hughes and the Tri-Service laboratories.

Five milestones have been completed, including the growth, Q/A testing and start fabrication of comparative single and multi-wafer pHEMT structures.

1.3 Vertical Zone Melt Growth of GaAs

PERF. ORG.:	M/A-COM
KEY PERSONNEL:	John Vaughn, Cesar Maiorino, Doug Carlson
CONTRACT NO.:	N00014-91-C-2000
FUNDING:	$920,129
PERIOD:	10/90-12/92
COTR:	Richard L. Henry

OBJECTIVES/APPROACH: The objective of this contract is to establish a domestic supply of ultrahigh-purity, low-dislocation-density, IC-grade, large-diameter GaAs wafers for use in microwave and digital IC fabrication. The approach is to transfer and scale to 3-inch diameter the Vertical Zone Melting technology developed at NRL.

GaAs device performance and yield are reduced by nonuniformities in the crystalline and chemical composition of the GaAs substrates used to manufacture discrete devices and integrated circuits. Improvement in the uniformity of the GaAs wafers would translate into improved capability and lower cost for many electronic systems. Vertical Zone Melting (VZM) is a new and versatile method of growing GaAs crystals of exceptional quality and uniformity. In VZM growth, the GaAs is drawn through a hot "spike" zone created by a computer-controlled multiheater furnace. The spike zone is bordered by other heaters (guard zones) which maintain the entire grown crystal at a nearly uniform temperature. The spike zone melts only a narrow band under a shallow, very carefully controlled temperature gradient.

For VZM growth, the solid-liquid interface is very nearly a plane, which promotes good yield of single crystals and, along with the shallow temperature gradient, results in a low and uniform dislocation density and a uniform EL2 concentration throughout the crystal. In addition to growth of highly uniform semi-insulating GaAs, VZM technology permits zone leveling of dopants to improve the uniformity of carrier concentrations/electrical properties from wafer to wafer and also permits zone refining to reduce the concentrations of unwanted impurities.

PROGRESS (Source: R. Henry, 10/92): M/A-COM has had its furnace built to a scaled-up version of the furnace that was used successfully at NRL for growth of crystals with a diameter of 34 mm. The new furnace has been installed at M/A-COM and thermal probing is completed. Tuning of the molten zone size and shape has not been completed due to an unexpected problem with ampoule swelling. The diameter of the ampoule ballooned to the point where the ampoule became stuck in the furnace on several experiments. A longer ampoule with more free space did not solve

the problem. A thicker-wall ampoule (5 mm) will be investigated during the next experiment. Less severe swelling of the ampoule occurred during VZM processing of large-diameter GaAs by the Mellen Company under a related SBIR program. Ampoule swelling was not a problem for the 34-mm-diameter crystal growth at NRL.

1.4 MOCVD Process Technology for Affordable High-Yield, High-Performance MESFET Structures

PERF. ORG.:	Spire Corp.
KEY PERSONNEL:	Kurt Linden, Jim Daly, P. Moise
CONTRACT NO.:	N00019-89-C-0152
FUNDING:	$545,265
PERIOD:	7/89-3/91
COTR:	Gerald M. Borsuk

OBJECTIVES/APPROACH: The success of the MIMIC program depends upon the availability of low cost, high quality GaAs starting material. In particular, for certain high performance applications, epitaxial GaAs MESFETs have provided superior performance with regard to power output at high frequencies (160 GHz) and low noise performance at lower frequencies. Of the several methods available for producing epitaxial material, molecular beam epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD) have shown the most promise for being able to produce high quality GaAs in quantity. Under a MIMIC Phase 3 contract, Spire pursued the development of GaAs MOCVD manufacturing capability to address the need for low cost, high quality GaAs epitaxial material.

A new, large-scale MOCVD reactor has been developed which can deposit on 14 2-inch or seven 3-inch wafers simultaneously. The gas flow dynamics of the reactor has been investigated theoretically by computer modeling and experimentally by flow visualization ("smoke") tests. The results of epitaxial growth of GaAs single layers and MESFET structures have demonstrated that thickness and doping uniformities of ±3% and ±5%, respectively, can be readily achieved. In addition, buffer layer leakage measurements have been performed on MESFET structures that were deposited on substrates from a variety of domestic and overseas suppliers.

PROGRESS (Source: N. Bottka, 4/92): This contract is completed and a final report has been issued but not yet filed with DTIC. The most significant accomplishments of the program were the completion of all major modifications to the MOCVD apparatus and the demonstration of epilayer uniformity exceeding the program goals of 3% in thickness and 5% in doping, on 75-mm-diameter substrates. A series of experiments to qualify substrates and identify substrate preparation techniques was completed. A cost model showing that MOCVD MESFET wafers can be produced for as little as $700 or less using the modified reactor was developed. Eight FET wafers were produced for delivery to the Phase 1 contractor. The wafers exhibited Polaron doping profiles that raised concerns about possible buffer leakage. Spire worked to grow acceptable wafers by modifying the reactor growth conditions. Since the unusual doping profiles may have resulted from shortcomings in the C-V measurement technique, Spire asked the contractor to evaluate the wafers fully by fabricating and testing finished FET devices on them. This technical issue was not resolved in time to deliver the remaining wafers specified in the Statement of Work. Twenty-eight of the required 50 wafers

were grown and 26 delivered. Some device fabrication and related tasks were not completed because of the technical questions concerning the eight FET wafers. Spire continues to work on understanding FET doping profiles and controlling buffer leakage. Since completion of the program, 75-mm-diameter FET wafers have been supplied to several firms for qualification.

1.5 Process and Technology Enhancements for MBE Production of MIMICs

PERF. ORG.:	Varian Associates
KEY PERSONNEL:	Thomas L. Cooper, Ron A. Powell, John A. Perri, P.E. Luscher, S-L Weng, J.N. Eckstein
CONTRACT NO.:	DAAL01-89-C-0907
FUNDING:	$1,238,558 (includes Air Force funds)
PERIOD:	5/89-1/91
COTR:	R. Lee Ross

OBJECTIVES/APPROACH: The aim of this program was to develop three key technologies needed to advance the use of MBE for production of III-V compound semiconductor microwave/millimeter wave monolithic integrated circuits:

- Task 1: Development of an in situ growth monitor using near-threshold photoemission (PE) oscillation.
- Task 2: Establishment of techniques to improve wafer temperature measurements.
- Task 3: Demonstration of techniques to minimize the oval defects occurring in MBE-grown material.

PROGRESS (Source: Final Report, 4/91): This contract has been completed and a final report has been issued. The following progress was made in each of the three tasks defined above:

Task 1: Near-Threshold Photoemission Oscillations: Control of epitaxial growth rate is a necessary requirement for reproducible epitaxial structures. Currently this control is obtained by the periodic growth of calibration wafers using either Bayard-Alpert type ionization gauges as beam flux monitors (BFM) or the reflection high-energy electron diffraction (RHEED) intensity oscillation technique. Both BFM and RHEED oscillation techniques provide satisfactory results but neither is capable of monitoring growth rate during real time. The presence of the BFM excludes growth and RHEED oscillation measurements exclude wafer rotation (sample rotation during growth is used to obtain uniform epitaxial films). To eliminate these deficiencies, work was directed at investigating the use of photoemission (PE) intensity oscillations as a means of real-time growth rate monitoring. Like RHEED, the frequency of PE oscillations is proportional to the growth rate. PE oscillations, however, should be less sensitive to wafer orientation, which should allow use of the technique while the wafer is rotating. Measurements were carried out using a hydrogen-deuterium lamp and resulted in a PE oscillation signal superimposed on a large non-oscillating background. An improved apparatus with increased sensitivity was later constructed using a tunable dye laser and a biased coaxial

detector. Measurements were made to determine the existence of PE oscillations resulting from a narrow band of exciting photons near the PE threshold energy. The use of this near-threshold technique was used to measure the growth rate of GaAs epitaxial layers at a rate of 0.54 micrometers per hour at a wafer temperature of 600°C and wafer rotation of 4 RPM. The resultant growth rate was shown to be in agreement with RHEED measurements.

Besides demonstrating the capability to use this technique with rotating substrates, two other significant results were obtained. First, the dependence of measurable oscillations on noise from the Ga source was demonstrated. Second, evidence was obtained that photoemission electron oscillations depend strongly on surface chemical composition, which allows photoemission oscillations to be used as an adjunct to RHEED oscillations for MBE growth mechanism studies.

Task 2: Improved Wafer Temperature Measurement: The major objectives of this task were: (1) to improve the measurement of substrate temperature to better control the epitaxial process, and (2) to improve the ability to design wafer holders which would result in improved temperature uniformity during growth.

The major result of this task was the invention and development of a new technique for the measurement of wafer temperature during MBE growth. The new technique, called point-of-inflection thermometry (POINT), overcomes the difficulties associated with the use of thermocouples and pyrometers and measures wafer temperatures to an accuracy of approximately ±2°C over a temperature range from 200°C to 800°C.

POINT senses the light transmitted through the wafer from the substrate heater and determines the inflection point of the absorption as a function of transmitted wavelength near the absorption edge. The wavelength corresponding to the inflection point changes monotonically with the wafer temperature due to the change with temperature of the wafer bandgap.

Complete calibration curves for semi-insulating GaAs were generated. Data for determining errors due to wafer doping and thickness variations were determined. A model for the POINT process was generated and fit to experimental data. The ability to measure the substrate temperature accurately with epitaxial layers of AlGaAs and thin epitaxial layers of InGaAs was demonstrated. A brassboard version of the POINT instrument was used to demonstrate wafer temperature measurement during MBE growth of GaAs with substrate rotation at 5 RPM. The important application of POINT as a tool for designing wafer holders with improved temperature uniformity was demonstrated.

Construction and testing of a manufacturing prototype have been completed, and there are plans to insert POINT units into the mainstream MIMIC programs.

During the course of the contract, it was shown that the POINT data acquisition time could be decreased from approximately 30 seconds (which is the data acquisition time for the current models) to under 100 milliseconds with the use of a detector array. One-hundred milliseconds is fast enough to use POINT in conjunction with a temperature

controller. In certain circumstances, such as in GaAs on GaAs structures, POINT can potentially yield alloy composition information as well as temperature information.

So far, POINT has used the wafer heater as the light source. The temperature range could be extended to lower temperatures by the use of an auxiliary light source. Similarly, with the use of auxiliary light sources, POINT could be investigated in the reflection mode. So far, only GaAs and InP have been studied with POINT. Other materials, notably silicon and HgCdTe, are also candidates for POINT development.

Task 3: Morphological Defect Reductic n: Historically, a significant disadvantage of using MBE for production of epitaxial GaAs and AlGaAs material has been the existence of growth-related morphological defects in the epitaxial layers. These defects, ranging in lateral size from less than one micron to several microns, have been associated with particulates on the wafer, inadequate preparation of the wafer prior to growth and "spitting" from the gallium source attributed either to droplets forming at the exit orifice of the crucible or oxides contained in the gallium melt. The combined result of all of these effects is a typical defect density ranging from a few thousand per square centimeter to a few hundred.

The major objective of this task was to find methods and equipment to reduce the total defect density of a one-micrometer-thick MBE-grown epitaxial layer of GaAs on a GaAs wafer, grown at one micrometer per hour, to less than 10 defects/cm^2 for all defects greater than 1 μm in size. Toward that end, a new gallium source was designed which, when used with low-dislocation-density, epi-ready wafers and careful wafer transfer to minimize particulate generation, resulted in total defect densities between 20 and 100 defects/cm^2 routinely. These results are believed better than any defect densities achieved to date. Four of the new sources were shipped to MIMIC Phase 1 contractors for evaluation (one each to Martin Marietta and TRW and two to GE).

At the end of the contract period, 10 wafers were shipped to the contractor with defect densities completely meeting or exceeding the contract objective. These wafers represent the lowest defect densities ever reported and are better than typical defect densities found for wafers grown by MOCVD or MBE.

Two other significant results were achieved during the period of the contract which were beyond the contract objectives. These results are defect reduction in films thicker than one micrometer and defect reduction at growth rates greater than one micrometer per hour.

Large defects formed on films approximately one micrometer thick originate primarily from particulates and from the Ga source. Once these sources of defects are minimized by appropriate particle reduction schemes and appropriate Ga cell designs, low defect wafers can be grown.

For epitaxial layer thicknesses of approximately ten micrometers, however, large defect densities will still be obtained unless further precautions are taken. To reduce these defect densities, it is necessary to grow on wafers having low dislocation densities and to carefully optimize the As/Ga ratio and wafer temperature. By applying these techniques,

the growth of ten micrometer GaAs films with defect densities under 200/cm^2 was demonstrated.

Finally, the ability to enhance the growth rate of GaAs layers and still maintain an acceptable level of defects was demonstrated. Layers have been grown at two micrometers per hour with defect densities under 100/cm^2 and at five micrometers per hour with defect densities under 200/cm^2. The implication of this result on the future cost of epitaxial layers is significant because this increased growth rate can boost the throughput of MBE machines without raising the cost of the equipment.

A copy of the final report may be obtained from DTIC (AD-B159565).

2. MIMIC MODELING, COMPUTER AIDED DESIGN, AND MHDL

2.1 Accurate Active Device Models for Computer Aided Design of MMICs

PERF. ORGS.:	Compact Software (Prime), Gateway Modeling (Sub)
KEY PERSONNEL:	Reza Tayrani (Compact), Bob Anholt (Gateway)
CONTRACT NO.:	F33615-92-C-1038
FUNDING:	$421,110
PERIOD:	6/92-12/93
COTR:	Rick D. Worley

OBJECTIVES/APPROACH: The overall objectives of this program are to increase the accuracy of active device models, both for the computer-aided design of MMICs as well as for the prediction of device characteristics from the process recipe. A process and device modeling program for HBTs and a direct physics-based extractor for HBT small and large signal equivalent circuit parameters (ECPs) will be developed. Gateway Modeling will enhance the G-PISCES-2B program to allow the simulation of pHEMTs and HBTs. Devices will be characterized in order to determine the temperature dependence of the equivalent circuit elements for MESFETs, pHEMTs, and HBTs from MIMIC Phase 2 foundries over MILSPEC temperature range and will improve the active device models in SuperCompact and Microwave Harmonica for temperature prediction capability.

Knowledge of the temperature dependence of FET performance is vitally important both for MMIC systems designers and foundries. Many systems for DoD applications require MMICs to perform over the -55 C to 125°C temperature range without loss of sensitivity and accuracy. Because intrinsic FET maximum available gain values decrease by as much as 2 dB per 100°, the MMICs must be temperature compensated, and to accomplish this, accurate models of the temperature-sensitive FET ECPs must be used. For foundry MESFETs, this data is scarce, and it is virtually nonexistent for mm-wave suitable pHEMTs and HBTs.

The most promising way to characterize and model FET temperature dependencies is with FET equivalent circuits. Instead of concentrating exclusively on the temperature dependence of measured gain or raw S-parameter data, the proposed approach will seek to determine with good

accuracy the temperature dependence of all parasitic and intrinsic elements of the FET equivalent circuit. This has two important advantages:

- An accurately extracted, temperature dependent equivalent circuit is immediately applicable to mm-wave designs above the testing frequencies—for example at V- or W-band;
- The physics of the temperature dependence is illuminated, and this can direct future FET process modifications or novel temperature compensation approaches.

It is planned to obtain chips from the MIMIC Phase 2 foundries, make S-parameter measurements over a range of temperature from - 60 to 110°C, extract ECPs from the S-parameters, then derive temperature coefficients for those ECPs. The derived coefficients will then become part of the foundry design databases, and will be readily used by Super-Compact and Microwave Harmonica circuit simulators.

Process and device models for pHEMT and HBT technology will be expanded and developed under this program which will:

- Allow process and device engineers to optimize and adjust processes for better or required transistor performance.
- Identify the impact of process variations on device characteristics or analyze what step in the process caused device characteristics to go off target.
- Analyze the physical reasonableness of measured or extracted device characteristics.
- Identify essential physics that should be incorporated into the circuit modeling programs.

The process and device modeling programs for HBTs consist of three parts:

- A process and one-dimensional device modeling program which will allow layer structures and the device layout to be specified. This will also solve the Poisson and electron-hole current-continuity equations in one dimension in order to calculate several device characteristics.
- In cases where two-dimensional effects are important, such as modeling surface recombination and emitter crowding effects, the process modeling program will generate mesh and control files for device characteristics to be computed using G-PISCES-2B. Under this program, G-PISCES-2B will be enhanced to allow heterojunction HBTs and pHEMTs to be simulated.
- The PISCES analysis program, PANA, which extracts equivalent-circuit elements from the PISCES results, will be modified for HBTs.

These programs will be integrated with other Compact software and Gateway tools for the simulation of MMICs based on either MESFET, pHEMT, or HBT technology starting from either device measurements or the process recipe.

PROGRESS (Source: R. Tayrani, 9/92): Work is under way to:

- Provide robust, easy-to-use model extraction tools for deriving model parameters from dc and RF data, as well as guidelines or even test plans to take the right kind of data for a wide variety of HBTs, as well as pHEMTs and MESFETs.

- Identify any limitations in the present equivalent circuit models, and, if required, add elements to improve the accuracy of the high-frequency models.
- Modify the linear and nonlinear circuit simulators, Super-Compact and Microwave Harmonica to make use of new models.
- Provide model parameters to MIMIC Phase 2 foundries for use in their modeling programs, which may include programs from other vendors.

2.2 Advanced Device Models for CAD in MIMIC Manufacturing

PERF. ORG.:	Gateway Modeling Inc.
KEY PERSONNEL:	Robert E. Anholt
CONTRACT NO.:	F33615-89-C-1049
FUNDING:	$223,469
PERIOD:	5/89-5/91
COTR:	Rick Worley

OBJECTIVES/APPROACH: One of the primary factors needed to assure the success of first-pass designs of monolithic microwave as well as digital integrated circuits using GaAs MESFET technology is good, well-understood measurements of device characteristics for use in circuit modeling. The role of the process and device simulator in design and manufacturing is to help provide that understanding. Gateway Modeling has developed several tools to provide a guide for:

- Understanding FET physics.
- Identifying elements limiting performance, thereby illuminating the pathway toward achieving higher-performance transistors.
- Understanding the relationship between process and device characteristics, allowing process engineers to concentrate on improving processes that most affect device uniformity.
- Understanding the essential physics that should be incorporated into circuit-model curve fitters, leading ultimately to increased accuracy for first-pass designs.

Gateway Modeling brought to bear several tools to meet these needs, including:

- GATES: A process and device model for GaAs MESFET technology
- GATES-2d: A two-dimensional Poisson solver for GaAs MESFETs
- G-PISCES-2B: A Poisson and current-continuity equation solver for GaAs MESFET technology
- SPECIAL: An S-parameter equivalent-circuit analyzer for the analytical extraction of FET model parameters from complex S-parameter data.

PROGRESS (Source: R. Worley, 10/92): This contract is completed and a final report has been issued. The main accomplishment of this work was the development of more accurate physical models and extraction techniques for GaAs MESFETs. The final report details the bias dependence

and theory of all of the equivalent circuit parameters for GaAs MESFETs operated in either the linear, saturated current, or breakdown regions. The temperature dependence of the parameters and noise parameters are also reported. The statistical validity of the equivalent circuit model for predicting microwave integrated circuit yields was investigated. With the aid of the GATES process and device modeling program, the root process variations were extracted from dc and RF data using a high density test mask fabricated under the MIMIC Task 4e program, and the relationship between process variations and variations in the FET S-parameters which affect MIMIC yields was investigated as well.

A copy of the final report may be obtained from DTIC (AD-B162721).

2.3 MIMIC Hardware Description Language (MHDL)

PERF. ORG.:	Intermetrics, Inc.
KEY PERSONNEL:	Pamela Stearman, David L. Barton
CONTRACT NO.:	DAAL01-91-C-0105
FUNDING:	$612,941
PERIOD:	11/90-2/93
COTR:	Lorna Savage Carmichael

OBJECTIVES/APPROACH: A hardware description language (HDL) is a formal language, much like a computer programming language, used to describe electronic hardware. This class of languages includes simulation languages like SPICE, Verilog, MAST and VHDL, and data exchange languages such as EDIF.

This contract is currently pursuing the development of an HDL with the capability of describing analog electronics with particular emphasis on the radio frequency (RF), microwave, and millimeter wave domains. There are two overall operational objectives: free exchange of information among engineers working on the performance and design of electronic systems, and a quantum advance in the system simulation capabilities available to these engineers. The long-range objective of this project is the attainment of a standard which commercial CAE vendors support.

The project is in the second of five intended phases: Requirements, Design, Demonstration, Standardization and Validation. Originally the cited contract covered only the first two phases but has since been modified to include the demonstration phase. Raytheon Missile Systems Division is a subcontractor to Intermetrics, assisting in the formulation and analysis of hardware description issues in this frequency band. Several other contractors are involved as well, together forming an MHDL Working Group, representing various disciplines that impact the development of the language.

The overall approach to language design taken here calls for: (a) capturing the state of practice in system engineering in a set of scenarios documenting the engineering practice, (b) analyzing the information content of the work products and inter-engineering messages occurring in these scenarios, (c) synthesizing a formal text language in which it is convenient to program a definitive statement of the information that must be conveyed, and (d) defending the decisions made

in the language design with the aid of application scenarios rewritten to show how messages and models written in MHDL would improve the efficiency and effectiveness of the engineering process.

PROGRESS (Source: P. Stearman, 6/92, and D. Barton, 9/92): Requirements for a MHDL were defined during the first phase of the program. Consensus on the requirements by the MHDL Working Group was reached gratifyingly quickly and published in the MHDL Requirements Document in October 1991. Concurrently, Intermetrics studied the feasibility of building a language based on VHDL and other CAD languages/formats. It was concluded that due to the range and type of information required by MIMIC designers, a language designed for microwave and RF applications could not be developed as an extension, super-set, or variation of VHDL. Mathematical complexity, large variations in the scope and representation of the information and complex relationships between different parts of the design information were some of the key issues which led to this conclusion. However, it was determined that it was feasible to define MHDL in a separate form that would still be capable of exchanging design information with VHDL for full electronic system support.

Actual development of the MIMIC Hardware Description Language began in November 1991 and is now (9/92) two-thirds through the language design phase. The major portions of the language have been identified and defined, and are in the process of being documented in the Language Reference Manual (LRM). Final copies of the LRM as well as copies of the preliminary LRMs and minutes of the Working Group meetings are available from Lorna Carmichael at US Army LABCOM, Ft. Monmouth, New Jersey.

The language that has emerged as a result of the deliberations of the Working Group is an innovative combination of features designed to permit the description of a broad range of microwave and analog systems. The language treats a microwave system as a hierarchical decomposition of parts. Each part is defined by a model, which may define both the structure of the part and the behavior of the part in the overall microwave system. The anchor of a model is a module, which contains basic definitions concerning the model. For example, the module of a model for a transmitter might define the parameters of the transmitter, such as gain, power consumption, etc. Each module may be altered or augmented by a number of modifiers. The modifiers contain those definitions that may or may not be shared by all the parts in the system of that particular type; for example, two different transmitters might have different implementations, and therefore might consist of different components.

The structure of the system is represented by an MHDL structure, consisting of one or more connections that specify the interface to the outside world, zero or more components, definitions associated with the components, and a connection map which describes how the components are interconnected. Each component names a model that describes the portion of the microwave system associated with the component.

The behavior of the MHDL code is represented by a series of signals relating to the information at specific connections in the MHDL description. Each signal can be either fairly simple or extremely complex, with multiple components of information. The building blocks of these signals are functions which describe the relationship between the independent and dependent variables of the function. These functions can be specified in a number of ways, including mathematical representations and executable functions.

MHDL descriptions can potentially provide information to a wide range of simulators and analysis tools. The flexibility of the language structures permits the models to be described in an implementation-independent fashion as much as possible, and implementation-dependent information can be segregated in separate modifiers. The total language gives the microwave designer wide flexibility in the description of microwave systems and components.

Intermetrics continues to test, analyze, and reanalyze the portions of the language already designed by codifying microwave design examples. The MHDL Working Group continues to provide key support by reviewing and critiquing the language and its features and by submitting microwave design examples.

2.4 Statistical Design Methodology

PERF. ORG.:	Motorola Inc.
KEY PERSONNEL:	Graham Bullock, Craig Fullerton
CONTRACT NO.:	DAAL01-92-C-0254
FUNDING:	$497,000
PERIOD:	6/92-6/94
COTR:	David Rhodes

OBJECTIVES/APPROACHES: Motorola's Government Electronics Group is presently producing large quantities of Ku-band transceivers for ALTAIR™, a commercial in-building wireless local area network, and will extend the Statistical Design Methodology (SDM) developed on that program to the broadband applications and advanced processes being addressed by the Raytheon/TI MIMIC Phase 2 team.

SDM does not duplicate existing CAD tools, but rather combines their capabilities with those of statistical design tools to provide a statistically based MMIC design approach that produces the most robust and lowest cost design possible. The designer obtains the statistical distribution of each performance characteristic by evaluating equations rather than by the use of random Monte Carlo analysis. He uses Design of Experiment (DOE) techniques for the development and evaluation of these equations. This program will develop software that automates the tools used in STM pursuant to ensuring successful first-pass designs of MIMIC subsystems.

The application of Motorola's Statistical Design Methodology to power and low noise amplifier designs developed, fabricated, and tested by the Raytheon/TI Phase 1 team will seek to validate the results predicted by the methodology. This effort will continue with the development of statistical models for the new Phase 2 processes that are different from the processes used on the Phase 1 designs. After this activity, Motorola will apply SDM to selected Phase 2 designs. The company will then provide the Raytheon and TI MIMIC designers with recommended modifications to improve their chip yield and provide a lower chip cost.

Motorola will work very closely with the Raytheon and TI designers in all aspects of this Phase 3 program, including training and consultation, to ensure the integration of SDM into their Phase 2 program. This program will also provide training and consultation for the GE/Hughes and TRW Phase 2 teams.

PROGRESS (Source: Technical Reports, 10/92): This program is expected to provide four major benefits: (1) it will expand Motorola's baseline Statistical Design Methodology, (2) the MIMIC community will have a validation of the Statistical Design Methodology, (3) the MIMIC Phase 2 designs will be given a statistical base, and (4) the unit cost of MMIC-based products will be reduced because of these SDM methods.

Raytheon and TI have selected circuits using the pHEMT process for the Optimization Phase of the SDM program. TI has chosen a power amplifier and Raytheon will choose between a power amplifier and a low noise amplifier. Development of the automated SDM software has continued. In particular, the data flow definitions based on the software specifications are complete, as is the SDM working code for the data collection. This program collects the LIBRA output files generated by the Design of Experiment (DOE) MACROS into a single text file with the data separated by TABS. The spreadsheets use this text file to analyze the results of the DOE. This code works for both linear and nonlinear simulations. The working code for the Monte Carlo Equation is 95% complete. All the input/output calculations (as defined) are working. The calculation for the two-factor interaction is nearly complete. Effort on the DOE analysis working code is currently under way.

Motorola has evaluated the Raytheon and TI circuit files on its computer platform. The power amplifiers are being analyzed initially, with the low noise amplifiers to follow. TI is collecting statistical data for its low noise process and will provide Motorola with statistical models by the middle of November. The Parameter Definition task using the Raytheon and TI validation phase power amplifier circuits is complete. The parameter definition task consists of finding the process parameters that are most significant for the output response of each circuit. This task also insures that statistical models will be available. As a baseline, a traditional Random Monte Carlo simulation on both power amplifiers was made. Using DOE techniques along with the LIBRA simulator, the significant process parameters were identified for the power amplifier circuits. The parameter analysis task for the power amplifiers has been completed for the linear analysis of the circuits. The nonlinear simulations are under way for the power amplifiers. The results of that effort are still being evaluated.

The verification of the keyboard MACROS has been completed (used for generating the DOE simulations on LIBRA). There are 25 MACROS for Linear and Harmonic Balance simulation, for a total of 50 MACROS. All the existing spreadsheet files have been updated to include wideband frequency information for analysis of the MMIC circuits from Raytheon and TI. There are seven spreadsheets available for DOE analysis with up to 23 variables. Validation of the MACROS, COLLECTED-DATA, and spreadsheets was made by using known equations with distinct coefficients for each variable and combination of variables. The LIBRA MACROS, COLLECT-DATA program and the DOE spreadsheets were used for the linear analysis of the power amplifier circuits. This software allowed wideband frequencies to be added as well as automation of the process. The nonlinear DOE simulations are under way. The software that is developed will also be used for these tasks.

2.5 A Physical GaAs MESFET Model for Nonlinear Microwave CAD and Yield Analysis

PERF. ORG.:	North Carolina State University
KEY PERSONNEL:	Robert J. Trew
CONTRACT NO.:	DAAL01-89-C-0906
FUNDING:	$198,014
PERIOD:	4/89-4/91
COTR:	Lorna Savage Carmichael

OBJECTIVES/APPROACH: The development of sophisticated computer-aided design tools for microwave integrated circuits is limited by the availability of accurate models for the GaAs MESFET. Severe restrictions are placed upon the simulator by the necessity of interfacing the active device model to linear RF circuit simulators. This requirement is easily satisfied for linear, low noise applications, but for nonlinear, large-signal circuits the requirement places severe limitations on the type of device simulation technique that can be employed. For example, all commercially available microwave simulators contain device models based upon equivalent circuit techniques. These simulators are suitable for circuit design applications, but require that the device be fabricated and well characterized before its use in a circuit can be investigated. This, of course, precludes device design optimization studies. It is difficult to relate the equivalent circuit elements to the actual physical structure of the device and, for this reason, these models are difficult to employ in performance or process yield simulations. Physical device models that relate MESFET terminal performance to device structure and design data offer significant advantages compared to the equivalent circuit techniques. Many physical models of varying complexity have been developed and reported and these models are ideal for detailed investigations of operational physics. The models consist of solutions to a set of the basic semiconductor equations under certain defined operation and boundary conditions. The equations are generally solved using numerical mathematical techniques and since the equations are time dependent, time domain solutions results. Unfortunately, due to lengthy execution it is difficult to obtain other than dc or transient solutions. It is very difficult to interface this type of model to RF frequency domain circuit simulators.

An attractive approach to the problem is offered by physical device models based upon analytic or quasi-two-dimensional solution techniques. These models can be efficiently formulated and when coupled with table lookup techniques produce a simulator that retains the accuracy of the physical approach while execution time is fast enough to permit direct integration with frequency domain RF linear microwave circuit simulators by means of the harmonic balance technique.

PROGRESS (Source: R.J. Trew, 3/91): This contract is completed and a final report has been issued. The complete simulator and User's Manual are available to the MIMIC community.

The NCSU large-signal MESFET simulator (TEFLON) was enhanced with an RF performance and process yield capability. RF performance and process yield are determined as a function of device design parameters that are actually accessible in the fabrication process. Equivalent circuit techniques are not required. The model calculates RF output power, power-added efficiency, gain, impedances, etc. as a function of device design data such as doping densities, geometry, and bias conditions. Yield is determined as a function of statistical variations in each of the design parameters. The model has been enhanced with integration of the Stanford SUPREM process model. This permits more accurate determination of channel doping profiles and allows optimization to be performed as a function of implant energy and dose, cap layer detail, etc.

Successful tests of the simulator for both RF performance and process yield application were performed. It was found that the simulator could be used to optimize a device design for a specified application (for example, maximum PAE under class B operation conditions) or used to "center" designs for optimum wafer yield.

A parameter extraction algorithm was developed for use in calibrating the simulator to experimental data. The parameter extraction procedure adjusts channel doping, charge carrier transport parameters, etc. until agreement between simulated and measured data is obtained. This algorithm permits more effective use of the simulator by design engineers.

The harmonic balance algorithm was significantly enhanced with advanced mathematical optimization routines. The simulator is essentially absolutely convergent for all levels of drive and RF saturation.

A variety of experimental devices from a number of MIMIC companies were simulated. The devices were designed to operate in C-band, X-band and Ka-band and had ion-implanted, uniform, and buried layer doping profiles. Both class A and class B operating conditions were considered. Excellent agreement between simulated and measured data was obtained in all cases.

A copy of the final report may be obtained from DTIC (AD-A242266).

2.6 Microwave Electromagnetic Software Applied to Massively Parallel Computers

PERF. ORG.:	Sonnet Software, Inc.
KEY PERSONNEL:	James C. Rautio
CONTRACT NO.:	N00019-92-C-0096
FUNDING:	$255,000
PERIOD:	9/92-9/94
COTR:	Denis Webb

OBJECTIVES/APPROACH: The purpose of this project is to port microwave electromagnetic software to two massively parallel computers: the Connection Machine and MasPar. The initial stages of the port will take advantage of readily available existing software, such as matrix inversion routines. Later stages of the port will emphasize custom written code to take maximum advantage of the characteristics of the particular analysis. The final stage of the effort will interface the capability to MIMIC workstation software. This effort will be assisted by Raytheon and GE.

To gain acceptance, software must be continually supported and updated, generally by the commercial organizations that created it. At present, there is no commercially supported microwave electromagnetic software on massively parallel computers because no one has considered it profitable to develop any. This program will seek to port an existing, commercially viable software product to massively parallel computers in the hope that the MIMIC contractors will then prime the pump of commercial viability for electromagnetic microwave software on such computers. This could lead to a cascading effect, enhancing prospects for not only commercial software vendors, MIMIC manufacturers, and massively parallel computer vendors, but also for related fields, such as high speed digital design, where this type of technology is becoming increasingly important.

While Maxwell's equations have been available for over 100 years, it is only in the last two years that electromagnetic microwave design software has become commercially viable. Properly used, electromagnetic software can eliminate the fabrication portion of the design-fabricate-measure-design cycle. The repeated fabrication of MMICs accounts for a major portion of the nonrecurring costs (both time and money) of MMIC design. For example, a month-long, multi-thousand-dollar wafer fabrication can be replaced with a few runs on a workstation-class computer.

Another reason electromagnetics has become important in MMIC design is circuit compaction. Since electromagnetics includes all possible coupling between circuit elements, accurate analysis of tightly packed circuits is easily accomplished. Thus the designer, by repeated analysis and redesign, can tune a circuit to achieve desired performance, including all interactions, without ever once fabricating the circuit. Circuit compaction of up to four times—that is, four times the number of chips per wafer—is readily achieved.

The present bottleneck in electromagnetics is caused by the fact that everyone wants to design circuits larger than present computer/software combinations permit. One potential answer is porting of software to large vector processors, such as the Cray supercomputer. This approach has been only partially successful.

Most electromagnetic analysis can be divided into two main phases. First there is the matrix fill, followed by the matrix solution. In the software ported to the Cray Y-MP and Cray X-MP, it was found that the matrix solution is an easily vectorized operation and can readily achieve about 200 MFLOPS (Million Floating Point Operations Per Second) performance per processor, close to the maximum capability. Unfortunately, the matrix fill operation is not easily vectorized. Typical performance is about 5 MFLOPS. This is equivalent to a high-end workstation.

Since, for large problems, the matrix solution dominates, the CRAY class of solution can become appropriate, though it is far from an ideal solution. Another possibility is the massively parallel computer approach.

Porting to the CRAY was facilitated by easy availability and because only minimal changes were required in the source listing. The same is not true of massively parallel computers. An extensive rewriting of code is required.

PROGRESS (Source: D. Webb, 1/93): Sonnet has ported its electromagnetic software, *em*, to MasPar machines. The specific model being used is a Northeast Parallel Architectures (NPAC) 64 by 128 MP-1 machine. Benchmark test results have been conducted on an *em* analysis of a microwave circuit. Because the front-end DEC 5000 Workstation at NPAC has only 16 megabytes (MB) of memory, the circuit size that can be analyzed by *em* is somewhat limited. The circuit being analyzed has 1325 sections (matrix size) and uses about 8 MB.

A principal conclusion from this test was that the overhead time (to initiate a data transfer between the front end and the back end) is significant. For the matrix fill operation, such an initialization must be done for each FFT. In fact, it takes less time to do actual computing than data transferring. In comparing overall MasPar computation time with that of a stand-alone DEC 5000 Workstation, the matrix fill operation was about the same for the two machines while MasPar achieved nearly a sevenfold speedup on matrix inversion.

These initial tests suggest several performance-enhancing possibilities: (1) make use of the symmetrical properties of the matrix for inversion to reduce memory requirements, (2) use 2D FETs instead of multiple 1D FETs, and (3) move entire portions of the matrix fill and matrix inversion operations into the MASPAR data processing unit to increase speed and alleviate the current memory burden (256 MB for the MasPar machine versus 16 MB for the workstation).

2.7 Modeling and CAD Methodology for Layout Optimization

PERF. ORG.:	University of Colorado
KEY PERSONNEL:	David C. Chang
CONTRACT NO.:	N00019-89-C-0151
FUNDING:	$676,287
PERIOD:	6/89-6/91
COTR:	Gerald M. Borsuk, Ken Sleger

OBJECTIVES/APPROACH: The objective of this project was to develop versatile multi-approach layout simulation tools for planar circuits. The effort involved the following key steps:

- Partition of a circuit configuration into individual sections, subsections and basic building blocks.
- Use of a full-wave moment method to extract the scattering matrix of individual circuit building blocks in isolation.
- Devising a multi-port connection scheme to produce an overall scattering matrix for interconnected circuit blocks and subsections.
- Application of the adjoint network/operator method to conduct sensitivity analysis that takes into account parasitic coupling of adjacent circuit sections.

The advantage of such a perturbative/iterative approach is that it converges quickly and is capable of minimizing the redundancies inherent in any circuit construction. Furthermore, it is easily adaptable to various concurrent computing schemes.

PROGRESS (Source: K. Sleger, 4/92): This contract is completed and a final report has been issued. Simulation tools have been developed and tested on double-stub and band-pass filters, interdigitated capacitors, microstrip serpentine lines, closely spaced power dividers and operational MMICs. A summary of the final report follows:

The planar waveguide model and the multiport network model (MNM) approach have been used to develop an algorithm for incorporating parasitic couplings in microstrip circuit analysis. The adjoint network method has also been used with this model to provide sensitivity analysis for parasitic coupling. The methods proposed have been generalized to make them applicable to a complete MMIC layout. An electromagnetic model that uses potential integral equations (called D-mesh) has been incorporated into commercially available software. A planar model for microstrip via hole grounds has been developed but is presently limited to cases where the post diameter is close to one-third of the pad width.

A copy of the final report may be obtained from DTIC (AD-B159578).

3. ON-WAFER TESTING AND AUTOMATED TESTING TECHNIQUES

3.1 MIMIC On-Wafer Chip and Module Automatic Testing

PERF. ORGS.:	Ball Communication Systems Div. (BCSD); Cascade Microtech; NIST; University of Arizona
KEY PERSONNEL:	T. Miers, E. Godshalk, D. Williams, A. Cangellaris
CONTRACT NO.:	N00019-89-C-0150
FUNDING:	$557,661
PERIOD:	6/89-4/91
COTR:	J.P. Letellier, G.M. Borsuk

OBJECTIVES/APPROACH: Ball Communication Systems Division's (BCSD's) MIMIC Phase 3 program addressed microwave and millimeter wave wafer measurements on GaAs. The two major tasks of the program involved: the development of interim NIST-traceable planar standards on GaAs and the development of 50-75 GHz wafer level probing technology.

Wafer level probing was used extensively by MIMIC Phase 1 contractors as well as by the GaAs MMIC industry in general. The measurement is fast and inexpensive and offers the promise of high accuracy. Unfortunately, there have been no traceable planar standards upon which to base these measurements. Because of the wide usage for modeling and performance verification, the largest part of BCSD's program was directed toward developing planar wafer level standards on GaAs that are NIST traceable. The objective of this portion of the program was to analyze planar standards/calibration techniques and develop a NIST-traceable interim planar verification kit for wafer level measurements over the frequency range of 0.045-26.5 GHz.

Millimeter wave probing to 50 GHz with analysis to 60 GHz was developed under the BCSD MIMIC Phase 0 program. This probing technology was based upon coaxial interfaces and has presently pushed coaxial systems to the limit. The 50-75 GHz probes being developed under the BCSD program represent a departure from coaxial interfaces to waveguide interfaces. This opens up not only higher frequency millimeter wave probing possibilities, but also potentially much more accurate measurements in the millimeter wave spectrum. The object of this task of the program was to design and fabricate millimeter wave probe heads for wafer level MMIC testing in the 50-75 GHz waveguide band and demonstrate this capability.

PROGRESS (Source: T. Miers, 4/92): This contract is completed and a final report has been issued.

The planar standard development task has been very successful. Coplanar waveguide standards on GaAs for wafer level calibration and verification have been developed. These standards are NIST traceable. The standards include transmission lines, opens, shorts and planar loads. Microstrip standards have also been developed. This work has led to an increased understanding of the loss and impedance of transmission line structures on GaAs and methods of calibration and measurement of monolithic integrated circuits at microwave and millimeter wave frequencies. Characterization, calibration and verification structures have been developed and measured. These structures allow the determination of physical and electrical parameters, highly accurate network analyzer calibration and calibration verification at the wafer level.

The second task, development of V-band (50-75 GHz) wafer level probing, has been completed. This effort required the design and development of waveguide-to-coplanar waveguide transitions at millimeter wave frequencies. These designs have been successful at solving the difficult requirements/issues of bias injection, low frequency impedance presented to the DUT, calibration, radiation/molding and mechanical compatibility. The V-band probe head developed under this program is now offered as a standard product from Cascade Microtech. The part number of this V-band probe is WPH-500. Millimeter wave S-parameter measurements on 0.1 μm pseudomorphic HEMTs using this probing technology have been demonstrated.

A copy of the final report may be obtained from DTIC (AD-B165643).

3.2 110 GHz Wafer Probing

PERF. ORG.:	Cascade Microtech, Inc.
KEY PERSONNEL:	Edward M. Godshalk
CONTRACT NO.:	DAAL01-92-C-0245
FUNDING:	$337,234
PERIOD:	4/92-4/93
COTR:	R. Lee Ross

OBJECTIVES/APPROACH: The objective of this program is to develop a W-band (75-110 GHz) wafer probe, including necessary calibration standards. The probe will have a waveguide input and be broadband in nature to allow full coverage of the 75-110 GHz range without tuning. To allow for vector-corrected measurements, a return loss of at least 8 dB and an insertion loss of less than 4 dB are desirable. An additional requirement is that the probe should allow biasing of active devices via a bias tee integral to the probe itself. Two industry partners, TRW and GE, are participating in the development of the calibration standards and evaluation of the wafer probe.

A probe similar in nature was developed by Cascade Microtech under a Navy MIMIC Phase 3 contract for coverage of the V-band (50-75 GHz). The V-band probe made use of a ridge-trough waveguide which can be fabricated to have a 50 ohm characteristic impedance and a coplanar electric field distribution. The ridge-trough waveguide was joined to a 50 ohm coplaner wafer probe board to allow transmission of millimeter wave signals from one medium to the other. The other end of the ridge-trough waveguide was joined to a rectangular waveguide via a carefully designed transition. The V-band configuration will be modified for use at W-band in this program.

The V-band probe project did not require significant redesign of the coplanar probe board already developed by Cascade Microtech for use in 65 GHz wafer probes. However, for uses up to 110 GHz, a new probe board is required to meet the insertion loss goals. To investigate the loss mechanism at W-band, transmission line models were made twice as large as the intended final versions and tested to 50 GHz. This should model the behavior for the final versions to 100 GHz.

Theory predicted that radiation loss should be the dominant insertion loss mechanism, but this proved to be false. Instead, conductor loss was apparently the dominant factor. New probe board designs are in process that will reduce conductor loss and other suspected loss mechanisms.

The 2X model also allowed investigation of models that might exist in the .010-inch-thick alumina probe boards. No mode problems were observed in the data. This agrees with mathematical models that were also developed for this investigation. Based on these observations, it is concluded that boards up to .010 inch thick may be used to 100 GHz.

PROGRESS (Source: R. Lee Ross, 12/92): According to a recent monthly technical report, impedance standards have been designed and sent to TRW and GE for review, layout and fabrication. Standards are included for lumped element and transmission line calibrations. Both microstrip and coplanar structures are included. The GaAs wafers made at TRW and GE are 100 and 50 μm thick, respectively.

Functional probe boards have been designed and laid out for fabrication on alumina substrates. This data was formatted onto a GDS-II stream file from which masks have been made. Fabrication of the actual probe boards is nearly complete. Probe bodies have been designed based on the successful results of the S21 test fixtures. These probe bodies incorporate the rectangular to ridge-trough waveguide transition and hold the probe cards described above. The probe bodies are presently in the precision phase of matching. A finishing matching operation will follow, and finally the parts will be gold plated and assembled.

An additional approach for realizing a W-band waveguide input probe was undertaken. It uses a waveguide-to-coax transition—that is, E-field probe in a waveguide—with a probe tip attached to the other end of the coax cable. Prior experience with coax-based probes has shown that although they generally have less insertion loss than the conventional alumina probe board probes, they suffer from high crosstalk and unwanted modes due to significant radiation at the open end of the coax cable. This results in questionable accuracy and poor repeatability. The positive aspect of coax-based probes is that they are generally relatively inexpensive to produce.

A rectangular waveguide-to-coax transition was built and tested. This was accomplished by building two transitions linked by 3.5 inches of coaxial cable. The insertion loss from 75 to 100 GHz was consistent at 4 dB. Research suggests that almost all the loss is due to the coax cable, at 0.8 to 1 dB/inch. This would imply that each transition contributes about 0.25 to 0.6 dB loss. It is interesting to note that this is not too different from the rectangular waveguide to ridge-through waveguide transition, which was typically less than 0.7 dB from 75 to 110 GHz. Investigations will continue by putting a probe tip on the coax.

3.3 Optical On-Wafer MIMIC Characterization Techniques

PERF. ORGS.:	COMSAT Labs; University of Maryland; TRW
KEY PERSONNEL:	T.T. Lee, H.C. Huang, T. Smith, C.H. Lee, E. Chauchard, T. Joseph
CONTRACT NO.:	DAAL01-89-C-0905
FUNDING:	$759,435
PERIOD:	5/89-5/91
COTR:	Arthur C. Paolella

OBJECTIVES/APPROACH: The objectives of this effort were threefold: (1) Validate picosecond optoelectronic measurement techniques of S-parameters through the design, fabrication

and test of optical test cell structures that are monolithically integrated onto MIMIC chips. Optically obtained S-parameters were compared to those obtained from a conventional network analyzer and contacting coplanar waveguide (CPW) wafer probes. (2) Develop a prototype optical on-wafer test system preparatory to eventual commercialization as well as to support the optical technique validation effort. Hardware and software requirements were developed and calibration techniques enhanced. (3) Insert the optical on-wafer measurement technology into the MIMIC program through direct interaction with a MIMIC Phase 1 contractor (TRW) as well as through development of a technology transfer/commercialization plan that makes it available to the broader MIMIC community.

Conventional techniques for on-wafer MIMIC characterization using contacting (CPW) RF probe tips and a network analyzer incur shortcomings such as the high recurring cost of replacing probe tips and high probe losses and hence degraded accuracy at frequencies above 40 GHz. Although they provide greater reduction of parasitics than can be obtained in fixture measurements, on-wafer CPW probe measurements are still a contacting invasive technique and thus sensitive to operator alignment error and problems associated with uniformity of probe placement and pressure.

The proposed optical measurement approach attempted to overcome many of these limitations. The baseline approach used photoconductive switches for the broadband and millimeter wave signal generation and sampling along a planar transmission line, such as microstrip. The photoconductive switch was implemented as a shunted 10 μm gap along the microstrip line. The time domain incident, transmitted, and reflected waveforms of the device under test (DUT) were sampled and converted into frequency-domain S-parameters. A picosecond-duration, mode-locked Nd:YLF laser beam shorted the dc-biased photoconductive switch momentarily and produced a near-impulse-like electrical waveform on the microstrip line. It had a high frequency content that extended into the millimeter wave range as a result of the sharp rise and fall times achieved with the laser pulse. The electrical pulses traveled toward the DUT and were sampled at one of three ports in the time domain. Using Fast Fourier Transform (FFT) techniques, the sampled waveforms were translated into the frequency domain. The gain of the DUT was obtained from calculating the ratio of the DUT's output signal to the input signal. The reflection coefficient was obtained from the ratio of the incident signal and reflected signal.

In order to adequately resolve the incident and reflected waveforms for the reflection coefficient measurement, a minimum required distance to the input of the DUT was needed to prevent overlapping (superposition) of the forward-traveling and reverse-traveling signals. This requirement increased the area used by the S-parameter optical test structure.

A second approach, invented under the support of this program, was based on Z-parameter characterization. It showed greater promise for more compact structures. The Z-parameter technique measured both current and voltage waveforms at the input and output ports of the DUT, thus eliminating the need for the temporal separation between incident and reflected voltage waveforms. The photoconductive switches can now be placed in close proximity to the DUT and still provide full 2-port parameters.

PROGRESS (Source: R. Lee Ross, 12/92): This contract is completed and a final report has been issued.

The successful progress of microwave/millimeter-wave monolithic integrated circuit (MIMIC) development has resulted in the insertion of these components into various systems. The

yield from MIMIC wafer fabrication has improved significantly in recent years. However, the conventional coaxial/waveguide frequency-domain approach for testing gallium arsenide (GaAs) MIMIC chips is one of the major cost drivers for MIMIC production. This is especially true for devices and circuits operating in the millimeter-wave (mm-wave) regime. Therefore, a low-cost testing technique which allows on-wafer characterization of MIMICs before the wafer is diced into individual chips is essential.

In addition to the cost factor, the evaluation of these devices becomes more difficult as applications extend into the higher mm-wave frequencies, which require a transition from microstrip to waveguide. The conventional waveguide approach is inherently limited by the waveguide bandwidth, resulting in the need for multiple calibrations for different waveguide bands when measurements are made over a wide frequency range. Furthermore, the need for high-performance waveguide-to-microstrip transitions for each waveguide band requires careful assembly of the transitions and the MIMIC test block. Such an evaluation process is both time-consuming and expensive. In addition, oscillations may occur during the characterization of active devices that are not properly terminated with matching circuits.

Existing commercially available on-wafer testing systems for MIMICs employing coplanar waveguide (CPW) probes have provided useful performance data up to 60 GHz, although further performance verification is still needed for these mm-wave bands. While attempts are being made to extend the frequency of operation of these systems, several fundamental limitations still exist. Because the systems use special CPW probes, it is difficult to achieve a low-loss, impedance-matched probe at mm-wave frequencies. The operating life of such a mechanical direct-contact probe is usually quite limited, and a customized probe card is required for each set of microwave circuits on the wafer. Furthermore, the characterization of MIMICs based on the impedance-matching provided by a CPW probe becomes more questionable for system applications dominated by microstripline structures.

In this program, the team of COMSAT, TRW, and the University of Maryland realized several key accomplishments:

- Establishment of an optical characterization system.
- Demonstration of broadband S-parameter characterization using optical built-in test structures (BITs) integrated with MIMICs.
- Design of an optical BIT which fits in the same area as CPW-probe pads.
- Development of improved software for data acquisition and analysis, and investigation of software requirements for a production optical characterization system.
- Reduction of laser pulse length to 2.5 ps to extend the frequency band for characterization to 100 GHz.
- Characterization of pHEMT MIMIC amplifiers at 60 GHz (optional task).

The COMSAT, TRW, and University of Maryland team has now demonstrated that optical characterization of MIMICs has overcome the limitations of the existing systems. For example, a 60

GHz monolithic amplifier can be RF characterized from dc to 100 GHz in a single system setup using the optical technique. On-wafer characterization over such a broad frequency range would be highly impractical using conventional techniques. Therefore, the optical approach is even more important for evaluating MIMICs at 94 GHz or even higher frequencies, since no conventional on-wafer testing technique is currently available.

Under Task 1, Insertion into Phase 1 and Microwave Frequency Validation of Optical Measurement Techniques, and an optional no-cost extension task (replacing Task 2, the unfunded mm-wave frequency validation task originally proposed), the optical on-wafer characterization technique demonstrated excellent MIMIC characterization data from dc to over 100 GHz. S-parameter data was obtained using a variety of optical BITs and monolithic amplifiers:

- TRW MIMIC Phase 1 amplifiers with integrated oxygen-implanted optical BITs.
- Oxygen and hydrogen hybrid optical BITs of an early COMSAT design connected to monolithic amplifiers.
- Improved hydrogen-implanted BITs with pulse-shaping networks.

Frequency validation was extended to 60 GHz by characterizing an existing COMSAT 60 GHz, pseudomorphic, high electron mobility transfer (pHEMT) monolithic amplifier. The results show that the optical technique is particularly valuable at mm-wave frequencies. S-parameter characterizations were compared to S-parameter data using a test fixture including fineline waveguide-to-microstrip transitions. Good agreement between the two methods was obtained, confirming that a single waveguide band does not always provide a sufficiently large frequency range for adequate mm-wave characterization. The waveguide-to-microstrip transitions were not "de-embedded" from the measurement. Since the optical measurement was done with a much smoother transition from the optical BITs to the monolithic circuit chip, the optical characterization is believed to be the more accurate one.

Under Task 3, Automation and Software Development, existing software for use with the improved optical system setup was revised under the optical on-wafer MIMIC characterization techniques program. New characterization software was written to use the two-sampling-switch-per-BIT method. All software program listings are given in appendices of the final report. The software that must be developed along with a prototype commercial optical test station have also been identified and specified.

Under Task 4, Optical Test Station Development, test station design was studied. It was concluded that a practical test station for a MIMIC production environment could be commercially produced. It was estimated that it would sell for a price comparable to that of a CPW-probe test station incorporating an HP8510 network analyzer equipped for V-band characterization. The optical test station has the advantage of not needing any component changes to set up for different frequency bands, so it could be more cost-effective when MIMICs for many different frequency bands must be characterized.

In Task 5, Technical Approach Enhancements, it was determined that truncation of the time-domain signal reduces the dynamic range. This can also lead to artifacts, especially where both incident and transmitted signals are truncated. If the incident and reflected signals are separated by

time-windowing, the only way to avoid truncation of the incident signal is to place the sampling switch a prohibitively large distance from the MIMIC circuitry. The only alternative is to use at least two sampling switches per BIT. This, along with the experience in Task 1 and the no-cost extension task, has led to the improved optical BIT design. This BIT design requires very nearly the same area as a CPW-probe pad.

In summary, the optical on-wafer MIMIC characterization techniques program has shown that MIMIC characterization using optical probing and the associated BITs is a useful and practical approach to on-wafer microwave/mm-wave characterization. It is particularly advantageous for mm-wave characterization, and for very broadband amplifiers. Other potential applications are the characterization of multiport circuits such as mixers and couplers, oscillator circuits, and large-signal waveforms of nonlinear circuits.

A copy of the final report may be obtained from DTIC (AD-B166680).

3.4 Automated Pulse Power Testing of Power MIMIC Wafers

PERF. ORGS.:	M/A-COM; GE; Cascade Microtech
KEY PERSONNEL:	Nick Jansen, Jean Pierre Lanteri, Peter Ersland
CONTRACT NO.:	F30602-89-C-0039
FUNDING:	$884,973 (plus $93,990 of company cost sharing funds)
PERIOD:	7/89-1/91
COTR:	Mark Novak

OBJECTIVES/APPROACH: The objective of this program was to reduce the cost of GaAs power MIMIC device testing by increasing the level of automation for full power device electrical characterization and by performing this characterization as early as possible in the process sequence. To address this objective, an automatic on-wafer pulsed power test stand was developed for both in-process and final (nondestructive) dc and RF screening of MMIC power amplifier die. Measurements were made of: scalar RF power out (up to 4W min.), vector S_{11} and S_{21}, group delay (transmission phase) and concomitant dc parameters (V_{DS}, I_{DS}, V_{GS}, I_{GS}).

The measurements and modeling work performed on this effort were compared to those obtained from final fixture measurements. Specifically, it was planned to measure test FETs in process, amplifiers on the finished wafer, and amplifiers on carriers, as well as establish correlations. Round-robin testing of the demonstration vehicle was to be performed by M/A-COM and GE.

PROGRESS (Source: M. Novak, 5/92): This contract is completed and a final report has been issued. A test system has been designed and built which allows GaAs MIMIC power devices to be electrically characterized under full power conditions at the wafer level. This system was used to significantly reduce the cost and time required for MIMIC Phase 1 C-band HPA test vehicle validation test and production test (70 wafers at M/A-COM and 100 wafers at GE, each 3-inch wafer containing 191 available devices). The total test time/wafer was about 90 minutes as compared to several hours for 19 chips realized by carriers on the Hughes/GE Phase 1 team. In addition, on-wafer measurements of over 1000 C-band power amplifiers were completed using test software with the following capabilities:

- Multiple test capability with a single touchdown
  - Small signal
  - P_{in} vs. P_{out}
  - Pulse profile
  - Power vs. frequency
- Both vector and scalar measurements
  - S_{11}
  - S_{21}
  - P_{in}
  - P_{out}
  - P_{ref}
- Concomitant dc parameters
- Optional dc screening
  - I_{DSS}
  - V_P
  - V_{DSBD}
- Discrete frequency points
- Multiple input power levels
- Variable pulse widths and duty cycles
- Measurement of peak power at user-definable time in pulse
- Minimal number of points for increased measurement speed

The technology developed on this program has already made an impact on the cost of power MIMIC devices, and will continue to do so in the future. The usefulness of this test system has been recognized throughout the GaAs industry. Several GaAs MIMIC foundries plan to implement this testing capability in the near future. Essentially all of the instrumentation required is commercially available, the single exception being the high current dc pulse modulator designed and built by GE (an electrical schematic and parts list is provided in the appendix of the final report, however).

A copy of the final report may be obtained from DTIC (AD-B161093).

3.5 Automated MIMIC Wafer RF Test System

PERF. ORG.:	Scientific-Atlanta, Inc.
KEY PERSONNEL:	O. M. Caldwell, William L. Tuttle, Daryl Vaughan
CONTRACT NO.:	F33615-92-C-1037
FUNDING:	$1,556,711
PERIOD:	4/92-3/94
COTR:	Bradley Paul

OBJECTIVES/APPROACH: The objective of this program is to reduce the cost of high-speed testing on-wafer and at the chip and module levels by developing test hardware and software that will dramatically increase measurement speed. The payoff will be a substantial savings in production cost of MIMIC chips and modules. The approach is to develop and demonstrate hardware and software that will reduce present MIMIC chip and module test times by at least an order of

magnitude. The test systems to be developed are a Core System, Multiport Control Circuit Tester (MPCCT), Millimeter Wave Low Noise Amplifier Tester (MMLNAT), Frequency Converter Circuit Tester (FCCT), and a Pulsed Power Amplifier Tester (PPAT). The chips to be tested are all from the MIMIC Phase 2 program and will be tested at Scientific-Atlanta facilities as well as at the Phase 2 foundry production sites.

Scientific-Atlanta's approach to a general-purpose on-wafer test system differs extensively from the more conventional system architectures presently in use, which typically rely on standard laboratory test instruments commanded through an IEEE-488 bus. The proposed system will make minimum use of the IEEE-488 bus, focusing instead on the use of a high-speed instrument interface, 80486-based system controller, multi-tasking/multi-processing operating system, existing S-A Model 1795 receiver (for network analysis of up to 5000 S-parameters/sec), and multi-purpose instrumentation to provide spectrum and noise figure measurements.

The program is expected to provide two major results. The first result will be a comprehensive ensemble of RF hardware and software designs to enhance the state of the art of MIMIC testing. The second result will be the testing trials on a selection of MIMIC Phase 2 wafers. All details relating to system design, performance and test results will be available from DARPA to any interested qualified member of the MIMIC community.

The techniques developed under this Phase 3 program are planned to be commercialized into an enhanced product family based on the Scientific-Atlanta Model 2096 Core System. Specifically, the products will address the following high speed test applications at the wafer, module or multi-chip module assembly level:

- High power output devices
- Small signal low noise devices
- Frequency conversion devices
- Multi-port and multi-state devices
- Coordinated dc and RF testing
- Device modeling and design centering

Product features from each test application area could be selected to form custom front ends for the standard 2096 Core System test architecture. Potential users could define a particular front end design from the available applications and procure a high speed, low cost hardware and software solution tailored to a given set of test requirements. A common front end architecture and supporting modular software would allow rapid system reconfiguration at low cost.

PROGRESS (Source: W. Tuttle, 9/92): The test station is under construction at Scientific-Atlanta and information on existing and upcoming Phase 2 chips from the various Phase 2 teams is being compiled for selection of the target chips. A list of the Phase 2 chips under consideration is shown in the table below.

MIMIC Phase 2 Potential Target Test Chips	
MIMIC Phase 2 Chip	**Team**
X-VGSA	GE/Hughes
7-bit Phase Shifter	Raytheon/TI
7-bit Attenuator	Raytheon/TI
HPA	TRW/Westinghouse
X-Image Reject Mixer	TRW/Westinghouse
X-HPA	GE/Hughes
Q-Transceiver	TRW/Westinghouse
Ka-LNA	TRW/Westinghouse
Ka-LNA	GE/Hughes/Litton
20 GHz LNA & PA	GE/Hughes
44 GHz LNA, IPA, & PA	GE/Hughes

Specific chip parameters and test data on these and other chips are being gathered from the associated Phase 2 teams to ensure that the test station will satisfy the critical requirements. The current plan is for wafers of the target chips to be supplied to Scientific-Atlanta for testing in Atlanta. In addition, testing at selected sites is under consideration.

3.6 Non-Contact Wafer Probing

PERF. ORG.: Varian Associates
KEY PERSONNEL: Majid Riaziat
CONTRACT NO.: F30602-89-C-0040
FUNDING: $450,955
PERIOD: 4/89-7/90
COTR: Thomas McEwen

OBJECTIVES/APPROACH: This program was concerned with developing the necessary technology for on-wafer RF characterization of integrated circuits without the use of high-frequency contacting probes. The technique is an extension of electro-optic sampling to include on-wafer optical generation of CW microwave signals.

The program consisted of two development efforts. One was the monolithic integration of a microwave electro-optic source with the circuits to be tested. The other was the design and assembly of the optical test station capable of non-contact measurements. The laser beam used for

signal generation is modulated through its power supply for lower frequencies, and by beating two optical beams together for higher frequencies.

Electro-optic sampling systems for high-speed measurements of electrical signals are available at Lightwave Electronics for commercial use, and at Stanford University as a research tool. The available bandwidth is 100 GHz, expandable to 300 GHz with present technology. The available electro-optic probing systems for testing microwave circuits, however, require high frequency contacting launchers to excite an input microwave signal to the circuit under test. For high volume RF testing it is desirable to avoid all contacts to the wafer except for dc biasing. In this program an all-optical method was developed that is compatible with present optical samplers for the excitation of microwave signals on wafer. Three approaches were selected for implementation:

- The first approach involves the direct modulation of a laser diode at microwave frequencies. The modulated beam is detected by a fast on-wafer photodiode which provides the excitation signal to the circuit. Presently, commercial laser diodes are available with modulation bandwidths of 10 GHz. Fast detector circuitry compatible with the MMIC process needed for this technique was developed and integrated with microwave circuits under this contract. The advantages of this method are several fold: the S-parameters can be measured directly, frequency can be swept, and excitation frequency can easily be phase locked to the sampling pulses.

- The second approach involves the mixing of two optical beams on a photodetector on wafer. The frequency separation between the two light beams is the desired microwave excitation frequency. This approach allows a very broad frequency selectivity limited only by photodetector bandwidth. Microwave signal generation with this method has been demonstrated on this program. The sources used are compact, solid state, diode-pumped lasers manufactured by Lightwave Electronics.

- The electro-optic sampler generates an optical pulse length of a few picoseconds at a repetition rate of approximately 100 kHz. In the frequency domain this corresponds to a comb of excitation signals spaced 100 kHz apart with a total bandwidth of about 100 GHz. A spectrum analyzer display of the output gives the frequency response of the device under test. The pulse-train approach is used in this program to test the response of the photodetectors. This approach was not selected for all optical testing of monolithic circuits because of the strict requirement that the device remain linear at all frequencies within the band regardless of the incident microwave power spectrum.

PROGRESS (Source: T. McEwen, 4/92): This contract is completed and a final report has been issued. All-optical measurement of the gain of two types of microwave integrated circuits (a feedback amplifier and a distributed amplifier) successfully demonstrated the technique. The only physical contacts were made by dc bias probes to supply power for the circuit under test and an on-chip metal-semiconductor-metal photodetector. The optically measured gains compared favorably to independent network analyzer measurements using contact probing. The integrated photodetector needed for signal generation is process compatible with MMIC technology, occupies a small space on wafer, and requires no additional processing steps. Since the photodetector yield is high compared to MMIC yield, the all-optical test is potentially a practical, low-cost, production RF testing technique.

A copy of the final report may be obtained from DTIC (AD-B154152).

4. PACKAGING TECHNOLOGY

4.1 Military-Qualified Net-Shape Manufacturing Process for Lightweight MIMIC Packages

PERF. ORG.:	Ceramics Process Systems Corp.
KEY PERSONNEL:	Richard W. Adams, Bruce E. Novich
CONTRACT NO.:	N00019-92-C-0106
FUNDING:	$999,923*
PERIOD:	7/92-12/93
COTR:	Joseph M. Colussi

OBJECTIVES/APPROACH: Present and future airborne array radar modules demand a cost-effective and lightweight packaging solution, consistent with the following key system-driven module requirements:

Lightweight	≤ 3 g/cc
High Thermal Conductivity	≥ 170 W/m-K at 25°C
	≥ 130 W/m-K at 125°C
Similar GaAs/Aluminum CTE	6.5 - 10 ppm/°C
Precise Dimensional Control	± 0.001 inches linear
Precise Flatness Control	± 0.001 in/in flatness

The next generation of military radar systems will have to overcome opponents' use of low observable technology in offensive weaponry. Radar systems will be required to perform near-simultaneous search and track functions over large scan volumes for large numbers of targets. Target acquisition through multiple-beam apertures will be required. In addition, future targets will continue to exhibit decreasing radar cross sections in an increasingly sophisticated electronic jamming environment.

The radar system designer's solution to this problem is to use an active electronically scanned array (AESA) radar architecture. The optimum architecture for present and future threats is a solid state phased array radar that consists of active transmit/receive (TX/RX) modules behind each antenna radiating element. To counter the offensive threat with a high probability of intercepting the target, the future AESA radar will require high peak and average radiated power in the transmit mode over wide operating bandwidths. The highest possible efficiency from the radar will be required in order to minimize the large prime power required for this mode, and very low noise figure will be required by the receiver to circumvent the opponent's use of low radar-cross-section offensive platforms.

While Phase 1 of the MIMIC Program demonstrated the low-cost potential of GaAs MMIC chip technology for these applications, the low-cost compatibility of associated packaging and interconnection technologies remains to be demonstrated. To overcome the shortcomings of conventional packaging techniques that use machined housings of CTE-matched materials, techniques that make use of net-shape forming methods will be investigated during this program.

---

*Total program cost is $1,100,144. The government share is $999,923.

Although the development of lightweight ceramic/metal matrix composite microwave packages has experienced significant technical and cost challenges that have delayed industrial-scale fabrication, Ceramics Process Systems Corp. (CPS) and several key subcontractors have made significant recent progress toward overcoming the technical challenges. Working with TI under the AFWL-sponsored Advanced Microwave Packaging (AMP) Program, CPS has managed to combine injection molding with metal infiltration technology to fabricate net-shape ceramic/metal matrix composite housings composed of discontinuous silicon carbide particulate reinforced aluminum. Nickel and gold plating processes and low temperature brazing processes have been developed to convert the composite housings into packages. Aluminum/silicon carbide transmit and receive packages have been fabricated and delivered for system evaluation.

The AMP program has successfully demonstrated the technical feasibility for specification-compliant aluminum/silicon carbide composite package fabrication and assembly. This MIMIC Phase 3 program will now seek is to demonstrate applications feasibility for this packaging approach through package integration into strategic military electronic systems. Key product attributes to be evaluated include package performance, package reliability and package design-to-fabrication cost.

This MIMIC Phase 3 packaging program will be carried out in 3 phases. Phase 1 is focused on baseline process variability reduction to give an optimized process flow to enable improved product yields. Phase 1 will be completed in August 1993.

Phase 2 is focused on the development and implementation of efficient manufacturing systems to reduce the manufacturing cost per unit. Phase 2 will be carried out concurrently with Phase 1 and will be completed in August 1993.

Phase 3 will integrate the optimized process specification into an efficient manufacturing system to produce validation hardware which will then be delivered to the Raytheon/Texas Instruments MIMIC Phase 2 team for further integration into their radar and electronic warfare systems. Phase 3 will be completed in December 1993.

During the course of this MIMIC Phase 3 contract, CPS will work with and support several potential lightweight packaging suppliers with the objective of creating a multisource domestic lightweight packaging supplier base, necessary to meet the critical and evolving needs of the DoD and DoD suppliers.

PROGRESS (Source: J. Colussi, 12/92): CPS is coordinating its effort with MIMIC Phase 2 team members TI, Raytheon, Lockheed-Sanders and Teledyne, and with its vendor, P-Cast. Recent effort has focused on the following areas:

Materials development: The fabrication of Al/SiC composite material for this task has been completed. A total of 54 RX shells and 108 coupons were fabricated of nine compositions. These compositions included the aluminum types A356.2, 6063, and 1100, and SiC particulate content of 50, 58, 63 Vol%.

The objective of this task is to down-select the optimum Al/SiC composite material combination. Selection criteria include: (1) ability to fabricate fully infiltrated void-free composites, (2) thermal conductivity. (3) thermal expansion, (4) compatibility with Ni and Au plating, and (5) compatibility with assembly processes, including brazing and lid sealing.

The data collected for each of these selection criteria will be presented to the MIMIC Phase 2 team, and the optimum material composition will be jointly down-selected.

The quality of the infiltrated composite parts from P-Cast has been dependent upon the aluminum type and the SiC preform type. Most parts produced with aluminum types 6063 and 1100 have significant solidification-related shrinkage voids within the Al-skin layer at the surface of the composite parts. The presence of these voids is independent of the SiC preform type. The aluminum A356.2 appears to produce the best results for the infiltration casting process used by P-Cast.

Thermal diffusivity and specific heat were measured at Virginia Polytechnic Institute. These samples supplied to VPI were machined from the 0.06-inch thickness of the RX shells. The sample thickness for the diffusivity measurements varied between 0.050 and 0.056 inch.

The result is positive because the quality of the infiltrated parts was superior with A356.2. Specifically, the 50% SiC composites average 150 W/m-K, while the 58% SiC composites average 133 W/m-K.

Design Influence on Properties: Fabrication was completed for RX shell preforms at base thicknesses of 0.020, 0.060 and 0.100 inch at 58 Vol% SiC. These preforms will be used to evaluate the coefficient of thermal expansion as a function of composite and Al-skin thickness.

EW Design: Completion of the EW (B4 R Module) SiC preform tool is proceeding on schedule. Delivery of the tool is expected during week 50. Lockheed-Sanders has reported that fabrication of the multi-pin headers will require 12-14 weeks after vendor's receipt-of-order. Final assembly evaluation of this package design is expected in March 1993.

Multi-Cavity Preform Fabrication: SiC preform fabrication for the MIMIC Phase 3 program is currently a "bench-level" operation of the Quickset™ injection molding process. The intention of this task is to increase the throughput of this fabrication process. Analysis showed that the multi-cavity approach would not significantly reduce the overall part fabrication cycle time. Effort will be directed toward the fabrication of a high-throughput, single-cavity machine which could produce more parts per manufacturing shift. In addition, the tooling cost per product line could be lower than the multi-cavity approach, and the machine could be built with sufficient flexibility for product line changes. The single-cavity modeling machine will be built with manually driven, mechanically articulated motions. The design will have flexibility for future machine concepts. This effort will build upon previous machine fabrication work at CPS, but will also incorporate some new features tailored to the packaging shape factor. Initial design specifications have been reviewed and machine design has started.

Program Management: A purchase order was placed with Texas Instruments for plating and brazing processing services. A delay in the infiltration processing at P-Cast has caused a three-month slippage in the Materials Development Task. This will cause a delay in the deliverables due December 1993.

4.2 Advanced Multi-Chip Ceramic Package

PERF. ORGS.:	ITT Defense; Alcoa Electronic Packaging
KEY PERSONNEL:	Ronald Schineller, Ken Hoffman, A. Collins
CONTRACT NO.:	DAAL01-89-C-0908
FUNDING:	$766,547
PERIOD:	5/89-3/92
COTR:	Owen Layden

OBJECTIVES/APPROACH: This program was carried out by Alcoa Electronic Products (AEP), the ITT GaAs Technology Center and ITT Avionics. The overall objective of this program was to develop high-performance, multichip microwave packages which would be rugged, reliable and producible by commercial suppliers at low cost. The package was to be available in both standard versions and semi-custom versions. The semi-custom version forms an "Application Specific MIMIC Module"—that is, the interior layout of the package, as well as the input/output (I/O) ports, can be readily designed to accommodate a specific set of MMIC chips. This approach has been shown to result in a significant reduction in module assembly time and thus lower production cost. The standard type, fabricated in two sizes, is suitable for one to four MMIC chips plus associated circuitry.

The fabrication approach for the package was based on Alcoa's high temperature co-fired ceramic (HTCC) process. This process has been demonstrated to be very rugged and reliable, and capable of very high volume production at low cost. High temperature ceramics such as alumina have the advantage of lower dielectric loss than low temperature ceramics such as glass, although this advantage may be offset by the higher resistance of the metal used with HTCC for the buried layers. The challenge was to apply the process to high frequency (1 to 20 GHz) packages and to demonstrate excellent performance.

After a number of design and process iterations, a set of packages was fabricated and tested and exellent performance was demonstrated. Key features of these packages are as follows: (a) excellent electrical performance including low VSWR and low loss, (b) low thermal resistance (metal) base for incorporation of high power chips, (c) multilayer connectors reducing the number of wire interconnects and eliminating crossovers by use of buried bias lines, (d) customized internal footprint reducing module cost while improving module reliability, and (e) flexibility of design allowing multiple I/Os and choice of alternative metal bases.

PROGRESS (Source: Final Report, dated 31 March 1992): This contract is completed and a final report has been issued. Standard packages suitable for one to four MMIC chips and semicustom packages suitable for up to 10 MMIC chips have been designed, fabricated and tested, with excellent performance demonstrated from 0 to 20 GHz. These packages utilize high temperature, co-fired ceramic technology which produces reliable, rugged packages capable of high volume, low cost production.

In order to select a set of performance objectives which would represent the needs of the user community, a survey was conducted early in the program of known manufacturers of microwave components. A questionnaire was sent out requesting information on the desired features and requirements of microwave packages. Mechanical features included such items as size, number of I/Os, mounting configuration, etc. Electrical specifications included frequency band, impedance

match, insertion loss, etc. The results of this survey were used to generate the following performance goals:

- Frequency 0 to 20 GHz
- VSWR (Input and Output) 1.3:1 max.
- Insertion Loss (Input/Output Transitions) 0.3 dB max.

The key performance characteristics of a microwave package—namely impedance match and insertion loss—are determined primarily by the design of the input/output feedthrough. The feedthrough is the transition region where the signal is carried from the outside to the inside of the package. The small standard package has two RF I/Os and eight dc I/Os located along the top and bottom. The I/Os are all microstrip lines with the RF lines having an impedance of 50 ohms. The package construction consists of a metal base, several layers of dielectric (alumina) which contain different metallization patterns, and a metal seal ring. This assembly is fused together to form a single, hermetically sealed unit. A metal cover completes the hermetic sealing of the package.

From an electrical standpoint, the feedthrough requires transitioning from a microstrip transmission line on the outside, through the package wall where the metal ring above the line forms a stripline (or coaxial) medium, to the inside where it is again microstrip. The metal is grounded (shorted to the metal base) through a series of plated through (via) holes in the dielectric substrate; in the transition region the via holes effectively form the sidewalls of a periodic coaxial line.

Considerable design effort was expended to develop a well-mateched transition. The final design utilized a combination coplanar waveguide (CPW) and stripline transmission medium in the transition region. In this region, the ground planes on either side of the signal line are brought in close proximity to the signal line and the dominant transmission mode becomes coplanar. The region where the line width is narrow is underneath the metal ring, where the transmission medium is a combination CPW and stripline. The dimensions were chosen so that most of the electric fields terminate on the side (coplanar) ground planes, thus reducing the effect of the metal ground plane on top. The via holes connect the top ground planes, the coplanar grounds and the bottom ground plane together to form a single RF ground. This is very important in preventing unwanted (higher order) modes of propagation, and for providing high electrical isolation between inside and outside the package.

This design was first simulated using an electromagnetic (EM) simulator (Sonnet), and then feedthroughs were fabricated and tested. The simulated and measured performance was exellent. The return loss was better than -20 dB over the full band, and the insertion loss was less than 0.5 dB. This data represents the performance of a single transition—that is, either propagating into or out of the package. This is a more meaningful parameter than a measurement of a complete package, because typically the chips mounted in a package will provide significant isolation between the input and output ports. The above performance parameters can be used, for example, to calculate the effect of the package on the input match or noise figure of a MMIC chip at the input, or on the output match or power output at the module output. The feedthrough performance described above met all of the original program objectives. Consequently, it was selected for use in both the standard packages and the semi-custom packages.

All of the original program objectives were achieved, with one exception—namely, providing a U.S.-based commercial supplier of microwave packages. Alcoa Electronic Products worked with ITT to develop and produce these packages and had planned to become a commercial supplier. Unfortunately, Alcoa decided late in 1991 that the market potential for microwave packages would not support their investment, at least until about 1994. Consequently, a business decision was made to discontinue the microwave packaging activity until such time as the market position improves. It should be noted that the viability of the high temperature ceramic approach was demonstrated, both technically by the excellent performance achieved and commercially by the fact that Intel is using about 100,000 pin grid arrays per week for 80486 PC processors which use this same technology.

Based on ITT's positive results with its co-fired ceramic technology, together with the design principles developed on this program, the company highly recommends this approach for MMIC module packaging. Specifically:

- A preliminary investigation of low-temperature co-fired ceramic was made during this program and some advantages were identified. Therefore, continued investigation and development of this technology is recommended.

- The benefits of multilayer construction in reducing the complexity of chip interconnect was clearly demonstrated, but additional metallization layers are required for high gain and/or high isolation applications. Additional effort is recommended to develop the process and finalize design rules for the multilayer construction.

- An alternate commercial supplier for production of the microwave packages described here should be developed using both the high-temperature and low-temperature co-fired ceramic technology.

Copies of the final report will soon be available from DTIC.

4.3 Millimeter Wave Packaging

PERF. ORG.:	Martin Marietta
KEY PERSONNEL:	J.J. Steppan, V.T. Brady, J. Carraway
CONTRACT NO.:	DAAL01-92-C-0250
FUNDING:	$786,028
PERIOD:	6/92-5/94
COTR:	Ed Baidy

OBJECTIVES/APPROACH: The objective of this program is to develop and produce affordable millimeter wave (MMW) packaging that meets weapon systems performance and reliability requirements. The conventional method of producing housings calls for aluminum investment castings which require further machining, especially on the mirror-like finish required for waveguide performance. This further machining results in increased cost. Martin Marietta has investigated new approaches to produce affordable housings and has chosen a high-payoff process called electroforming. Electroforming is an automatic, controlled batch process wherein metals are deposited

and exactly replicate the shape and features of the mandrel. The electroformed part is then separated from the mandrel as a final package. This technology is low risk and offers inherent advantages, such as:

- The housing coefficient of thermal expansion (CTE) can be matched to GaAs, eliminating the need for copper-tungsten base substrates, thereby reducing assembly and rework costs.
- Highly polished surfaces suitable for waveguide applications can be produced directly without further machining or polishing.
- Complex, lightweight, strong, thin-walled structures can be produced to exacting tolerances.
- Both metallic and non-metallic inserts, such as coaxial feedthrough and waveguide windows, can be "grown" in-place, eliminating the need for further assembly.

Electroforming will provide additional assembly and rework savings because the waveguides are formed as part of the process. Electroformed parts usually require no additional machining or polishing. The need for copper-tungsten base substrates is eliminated, because the package is CTE-matched to GaAs, and coaxial and power feedthroughs are electrojoined as part of the process. All represent additional assembly cost when using investment casting.

The program will be conducted in seven tasks, defined as follows:

Task	Description
1	Electroformed MMW Housing
2	MMW Package and Substrate Design
3	Functional Demonstration
4	Reliability
5	Technology Transfer
6	Interface with Industry
7	Program Management

PROGRESS (Source: Tech Report, 10/92): The electroforming of Fe-Ni cylinders for the thermomechanical optimization studies (Task 1) has been initiated. The effects of bath chemistry, plating current and hydrodynamic conditions upon deposit composition and appearance are being calibrated.

Ten aluminum mandrels were fabricated for the waveguide loss/surface finish studies. Surface roughness measurements were performed with a noncontact optical profilometer; however, this technique only worked on the smoothest finishes. Thus, the surface finishes of the mandrels will be measured using a contact profilometer.

Several design concepts for the interim single-channel waveguide package (Task 2) and subsequent mandrel are being evaluated. The machining of five stainless steel (17-4) mandrel blanks and fixturing have been completed. The approach taken is first to electroform blank packages with no electrojoined features in order to optimize plating conditions, then to electroform packages with only waveguide transitions, dc feedthroughs, or threaded bosses in conjunction with electrojoining efforts. Finally, electroforms with all features will be produced. The mandrel for the final waveguide housing will be a multi-piece mandrel. This is necessary to electrojoin the dc feedthroughs in place and then be able to separate the mandrel from the electroformed package. Design of the substrates

that are needed to connect the chips to the transitions and provide dc to the chips has been initiated. The design of the connecting substrates will be finalized after the final design of the housing. Designs based on modifications of the waveguide housing for the coaxial housing were initiated. A new design to yield a smaller package for the coaxial amplifier housing was also designed for comparison.

5. ADVANCED PROCESSING

5.1 Focused Ion Beam for Gate Processing

PERF. ORGS.:	TRW; MBI
KEY PERSONNEL:	John Berenz (TRW), William Robinson (MBI)
CONTRACT NO.:	N00019-89-C-0149
FUNDING:	$616,942
PERIOD:	7/89-4/91
COTR:	Gerald M. Borsuk, Harry Dietrich

OBJECTIVES/APPROACH: This project improved techniques for fabricating GaAs field effect transistors (FETs). One of the most critical steps in fabrication is the gate recess etch. It controls both dc and RF parameters of the FET, such as the saturated drain-source current, I_{dds}, and the cutoff frequency, f_T. In the current art, this step is a wet chemical etch and therefore difficult to control at the microscopic level, leading to an undesirably wide spread in GaAs FET parameters and reducing circuit yield. This project sought to develop a highly controlled, reproducible dry process for gate recess etching of GaAs MIMIC devices.

Specifically, the aim was to develop and automate focused ion beam (FIB) etching techniques to recess FET gate structures. Potential advantages included improved uniformity, performance and yield of GaAs MIMIC die. Emphasis was on process validation and technology insertion. MicroBeam Inc. (MBI) performed the actual etching experiments; Lincoln Laboratory provided ion-beam assisted etching (IBAE), reactive-ion etching (RIE), and evaluation services; and TRW demonstrated the improvements achievable with FIB gate recess etching by processing the wafer in the company's pilot line and directly compared the results with the Phase 1 baseline approach.

Three approaches were investigated: FIB+IBAE/RIE/Cl_2; physical etching; and gas-assisted etching. The FIB+Cl_2 process was selected because of its superior physical characteristics and throughput advantage. A 3-inch GaAs wafer pallet was built and tested, along with test structures and FETs. The goal was a ±2.5% variation in FET saturated drain-source current over a 3-inch wafer.

The program had three parts: Part I, a 6-month study phase; Part II, covering demonstration, test and evaluation (12 months); and Part III, the insertion phase (4 months).

PROGRESS (Source: H. Dietrich, 4/92): This contract is complete and a final report has been issued. TRW and its subcontractor, MicroBeam, Inc. (MBI), have developed a novel in-situ dry

etching process that uses focused ion beam (FIB) exposure and chlorine (Cl_2) gas to etch the gate recess of GaAs FETs. The gate recess areas are patterned by direct-write FIB gallium (Ga^+) ion implantation to remove the GaAs surface oxide. The substrate is then heated in situ and chlorine gas is used to etch the GaAs recess in the exposed areas, removing the implantation damage. The result is a precisely controlled and damage-free recess ready for Schottky-barrier gate metal deposition.

Test structures and ungated FETs have been built which have successfully demonstrated the gate recess etching process. Software suitable for the automated etching of 3-inch wafers has been developed and installed. Uniformities approaching the 2.5% goal of the program have been measured. Test runs of MIMIC chips will be carried out on the TRW pilot line.

An extension of this program is the direct deposition of the gate metal by the focused ion beam technique, thereby eliminating several steps in the conventional process at a large potential production cost savings.

A copy of the final report may be obtained from DTIC (AD-B157628).

5.2 Heterojunction Bipolar Transistor Development for Advanced Low Power Circuits

PERF. ORG.:	University of California, San Diego
KEY PERSONNEL:	Peter Asbeck
CONTRACT NO.:	DAAL01-92-K-0262
FUNDING:	$122,359
PERIOD:	8/92-7/94
COTR:	Wayne H. Chang

OBJECTIVES/APPROACH: The objective of this program is to dramatically improve HBT technology. Toward that end, effort will be directed at reducing power dissipation in small signal circuits, increasing affordability, and improving power efficiency of HBTs for MIMIC Phase 2 circuits. The program is being carried out in close collaboration with TRW Electronic Systems Group, Redondo Beach, CA, and with Rockwell International Science Center, Thousand Oaks, CA (in conjuction with Hughes Aircraft Company). Investigation will focus on epitaxial structures and lateral structure modeling and design, HBT process experimentation and refinement, circuit design and circuit demonstration.

To improve HBT performance, the key requirement is to scale down the parasitic base-emitter and base-collector capacitances, Cbe and Cbc, which are the major factors limiting performance at low levels of power dissipation. To decrease Cbe and Cbc, it is important to reduce the device dimensions and employ advanced structures and fabrication techniques that reduce base-emitter and base-collector capacitances. These developments coincide with the requirements for reduced device and circuit size, thus increasing affordability.

In addition to communication, radar and smart weapon low power applications of HBT technology, another significant goal within MIMIC Phase 2 is the development of high power, high efficiency HBT-based power amplifiers. For these devices, the key limitation on performance in

wideband circuits is an issue closely related to that of low power operation. For efficient output matching over a wide bandwidth in a power amplifier, it is necessary that the output Q of the device not be particularly high (otherwise, through Fano's theorem, there is an unavoidable trade-off of bandwidth and degree of matching). The output Q is determined by the parasitic capacitance Cbc. Thus, the critical device improvement for power amplifier applications coincides with the required improvement in Cbc that is addressed in this program.

Specific program tasks include: (1) epitaxial layer design and optimization, and associated experimental demonstration; (2) HBT process development, including aggressive use of implants for capacitance reduction, novel structures which dramatically decrease base-collector capacitance, and scaling of device dimensions, particularly emitter width, and (3) demonstration of improved devices and their use in MIMIC chips with x2 reduction in power dissipation and x1.5 reduction in chip area.

As demonstration vehicles for the technology improvement, several MIMIC chips will be used:

- One demonstration circuit is an HBT chip that is presently part of the MIMIC Phase 2 EHF data-link brassboard under development by the TRW team. The HBT chip contains a VCO integrated with a frequency divider and buffer amplifier.

- Another demonstration chip is an HBT chip from the MIMIC Phase 1 MLRS-TGW brassboard demonstration by the TRW team. This HBT chip contains four amplifier stages followed by a frequency divider.

- The applicability of HBT technology to power amplifiers will be demonstrated utilizing an X-band power amplifier. A circuit whose design has already been verified in conventional HBT technology will be appropriately modified and fabricated alongside the other circuits. The impact of the reduced base-collector capacitance will be assessed.

The tasks of the proposed program will be carried out in two phases. In the initial phase, process development experiments will be undertaken to demonstrate the advanced devices and determine key characteristics to allow adequate circuit design. In the second phase, circuit layout, fabrication and testing will be accomplished.

PROGRESS (Source: Tech Report, 10/92): This program is directed towards HBT structures that minimize the critical parasitic capacitances Cbe and Cbc in order to obtain high f_t, f_{max} operation at low currents and low current densities, and in order to improve the performance of microwave power HBTs.

Progress has been made in the two initial tasks of the program: technology development to reduce Cbe, and technology development to reduce Cbc.

(1) Cbe Reduction: Epitaxial layer structures have been designed at UCSD which, according to simulation, reduce Cbe by more than a factor of five. The designs utilize a lightly doped emitter region (LDER). The calculated variation of f_t with current density for various LDER widths shows that dramatic improvements should be possible in comparison with the baseline structure. However, it was determined that if the LDER is too wide, current gain (beta) would drop. A method was devised to avoid the drop in beta while attaining further improvement in f_t by adding a delta-

doped layer in the emitter AlGaAs. The calculated effect of this delta-doped layer on f_t and band structure has been determined. The final band diagram and carrier concentration profile have been calculated.

Companion simulations were done to attempt to "validate" the simulation methodology by fitting characteristics of baseline TRW HBT structures. The simulations were "brought into agreement" with experiment in terms of beta and Vbe by adjusting lifetime and bandgap narrowing parameters. However, the base-pushout and collector transit times still could not be accurately described, perhaps because the SEDAN simulator lacks estimation of electron velocity overshoot. Nevertheless, the simulator does seem to perform adequately in describing the task's crucial features.

A meeting was held at TRW to discuss the HBT structures. The UCSD simulations were described and numerous constructive comments were made. It was jointly resolved to embark on a set of six experimental wafer growths (two of each of three different structure variations), to be carried out at TRW. These wafers will be subsequently processed into HBTs and circuits in baseline process lots (which will also include baseline wafers for comparison). The experimental wafers will be incorporated into two process lots to enable determination/analysis of any lot-to-lot variations.

(2) Cbc Reduction: The immediate objective is to establish an implant process that will allow extensive compensation of both the collector and subcollector layers of the HBT, while leaving relatively untouched the heavily doped p+ base of the device. With such a process, a self-aligned implant could be used to virtually eliminate the extrinsic component of Cbc. A promising implant profile to achieve this (dual energy helium implant) has been established. Standard HBT wafers were implanted at Rockwell to evaluate the process experimentally. Contracts were applied at UCSD in a Transmission Line Method pattern for resistivity measurement. Sheet resistance was measured after implant as well as after several heat treatment steps (performed sequentially on the same samples). Base and collector sheet resistances were obtained for the samples. Despite scatter and some effects that may be due to experimental error, the experiment shows that there is a regime where the base resistivity is increased only moderately (x2.5), while the collector resistivity is increased massively (by more than 10^6), as needed for the high performance HBT structure. The data suggest that an optimal dose is around $5x10^{13}/cm^2$, and that it is better to use a double-energy implant than a single-energy implant. These wafers will be further annealed to collect more data, and a second experiment conducted to confirm the results.

5.3 Low Cost Ion Implanted Millimeter Wave Monolithic ICs by Direct Ion Implementation into LEC GaAs Substrates

PERF. ORG.:	University of Illinois
KEY PERSONNEL:	Milton Feng
CONTRACT NO.:	F33615-92-C-1039
FUNDING:	$348,110
PERIOD:	4/92-10/93
COTR:	Ronald J. Schweller, Mark Calcatera

OBJECTIVES/APPROACH: The objective of this program is to develop and verify a millimeter replacement low noise amplifier (LNA) suitable for insertion into the Navy's Advanced

Multimode Missile System. This will be accomplished by optimizing techniques for direct ion implantation into gallium arsenide (GaAs) substrates.

Current design and fabrication approaches rely on HEMT technology. Unfortunately, both the design and fabrication of HEMT MMIC technologies are still relatively immature due to an incomplete understanding of the fundamental device physics, a lack of well-established HEMT models and undetermined scaling behavior. The critical dimension requirement (<40 Å) of the HEMT material structures creates yield difficulties for mass wafer production, reliable ohmic contacts and uniform gate recess etches.

In this program, the contractor will determine the optimal ion implantation schedule and optimal annealing condition for 0.1-μm-gate ion implanted GaAs MESFETs. Three alterations of these super-low-noise MESFETs will be evaluated. The noise figure will be evaluated from 3 to 18 GHz and the equivalent circuit model will be generated. The contractor will redesign the AAAM LNAs and process two iterations based on the optimization of the 0.25-μm-gate, ion implanted GaAs MESFET model. The goal is a 3.5 dB noise figure with 25 dB associated gain at Ka-band. Hardware, reports, and program reviews will be presented according to the program schedule for deliverables.

Current fabrication techniques for manufacturing high performance millimeter wave LNAs require epitaxy procedures that are very costly. Successful development of the proposed LNA using direct ion implantation would greatly reduce manufacturing costs for the GaAs industry in general and DoD systems in particular.

PROGRESS (Source: M. Calcatera, 10/92): Twenty implanted GaAs wafers from Raytheon as well as 14 GaAs wafers from Wright Laboratory were successfully annealed by the University of Illinois. These wafers were used to complete the optimization of the University's CAT Anneal Process. The sheet resistance values for the Raytheon wafers show good uniformity, with standard deviations between 1.5% and 3.0%. Results also show the sheet resistance increasing with increasing implanted acceptor dose. The University investigators hope to get Polaron profiles of the samples to further explore the results of the implant. The optimum low noise implant will be determined from this data as well as the electrical properties of the devices fabricated on these materials.

The first six wafers from Wright Laboaratory were annealed in lots of three, and the last eight wafers were annealed in lots of four each. The fourth wafer in each of the last two lots fell outside of control limits defined by the first six wafers. This change could be due to the thermal loading of the fourth wafer as well as the gas flow around the wafers. In either case, to attain the most consistent results, the University of Illinois investigators will continue to anneal in lots of three wafers each.

6. FOUNDRY FABRICATION

6.1 Foundry Fabrication of MIMIC Chips

PERF. ORGS.: Avantek; Westinghouse
KEY PERSONNEL: Robert M. Malbon, James L. Vorhaus, and Tina Ohlhaver (Avantek); Evan Deoul (Westinghouse)
CONTRACT NO.: F33615-90-C-1518
FUNDING: $2,955,154 (includes Air Force funding)
PERIOD: 10/90-1/93
COTR: Tony Quach

OBJECTIVES/APPROACH: The objective of this program is to demonstrate MIMIC technology support that has high payoff in terms of producing MIMIC chips and modules in a reliable, low-cost manner that can be integrated into the MIMIC Phase 1 and 2 programs. An important aspect of the program is the development of a high-volume, high-yield MIMIC foundry capability.

The program is divided into two tasks. During Task 1 the objective for the foundry was to collaborate with a systems manufacturer to design a high-interest chip set that would provide both high performance and low cost for a system insertion. Following this chip definition phase, appropriate mask sets would be procured and 50 3-inch wafers processed and fully characterized to ensure all design requirements were met.

During Task 2 the objective is the fabrication and testing of 250 3-inch wafers. A database is to be constructed to track yields, performance levels, performance variation and cost.

Avantek's approach called for collaboration with Westinghouse Electric Corp. in the development of a MIMIC chip set suitable for insertion in radar T/R module programs. The objective was to develop a generic chip capability that would permit the insertion of specific chips into a variety of X-band T/R module programs. Since the two most critical component functions in an active array T/R module are the power stage on the transmit side and the LNA on the receive side, these were the two component functions selected for MIMIC implementation on this program.

The baseline approach for the fabrication of the LNA MIMIC chip (designated the M262) was to take advantage of Avantek's pseudomorphic HEMT (pHEMT) technology to design a low-noise, high-gain, high-intercept-point MIMIC. To achieve the desired performance characteristics, the pHEMT device was fabricated using direct-write, electron beam lithography to define the gate dimensions. To ensure low parasitics, a 0.25 μm mushroom gate process was used.

The baseline approach for the fabrication of the power MIMIC chip (designated the M348) was to use Avantek's power MESFET process that takes advantage of a 0.4 μm mushroom gate process and a high-low-high (HLH) doping profile created by MBE. This profile provides an excellent combination of high cutoff frequency, high breakdown voltage and high output resistance. Avantek's MESFET process provides lower source inductance through the use of small chip thickness.

PROGRESS (Source: J. Vorhaus and R. Malbon, 9/92): The Task 1 efforts have been completed for both MIMIC chips. The power MIMIC chip was incorporated into a power module, 10 of which were delivered to WEC for more complete evaluation in a system application. In addition to the design and wafer fabrication tasks, on-wafer dc and RF probing techniques were developed to permit fully automated characterization of both the LNA and power MIMIC chips. For the LNA MIMIC, a key development was the evaluation of not only the gain and noise figure on wafer, but also the on-wafer evaluation of the third-order intercept point at the amplifier input. For the power MIMIC, a prematched power FET cell using a coplanar approach was added to the process control monitor (PCM) to permit RF power performance evaluation on wafer.

The table below summarizes the performance of the LNA MIMIC chip developed during the Task 1 efforts. The LNA is a two-stage design using a 300 μm gate periphery FET for the first stage and a 400 μm gate periphery FET for the second stage.

Parameter	Units	Targets	Performance
Frequency	GHz	8.5-10.5	8.5-10.5
Noise Figure	dB	2.0	1.6
Gain	dB	18.0	18.0
Input Third Order Intercept	dBm	+10.0	+6.2
VSWR	---	2.0:1	2.0:1
Voltage	V	6.0	6.0
Current	mA	90	90

The table below summarizes the performance of the M348 mounted on a test carrier for evaluation. The power MIMIC chip is a two-stage design using 2.75 mm of gate periphery in the driver followed by a 7.2 mm FET in the output stage.

Parameter	Units	Targets	Performance
Frequency	GHz	8.5-10.5	8.5-10.5
Power Output @ -2 dB	dBm	34.5	35.5
Gain @ -2 dB	dB	15.4	15.0
Power Added Efficiency	%	31.1	30
Voltage	V	9.0	9.0

During Task 2, the designs completed in Task 1 for both the LNA and power MIMIC chips are to be fabricated on 3-inch wafers and characterized on wafer. Due to the larger size of the power MIMIC, a larger percentage (≈75%) of the 250 wafers to be processed in Task 2 will be allocated to the power MIMIC chip.

To date, all 190 wafers of the power MIMIC have been started in fabrication. Of these, 170 wafers have completed topside fabrication. Of the completed wafers, 100 wafers have been evaluated for both dc and RF performance. For the LNA MIMIC chip, which was scheduled to start later in the program, more than 50% of the wafers have been fabricated to date.

A complete database has been structured for monitoring the dc and RF performance of the MIMIC chips in addition to the complete PCM data. More than 20 megabytes of data were delivered to AFWL to date.

In the design of the power MIMIC, particular emphasis was placed on flexibility and broad applicability to assure multiple potential insertions in the future. Accordingly, Avantek, with Air Force concurrence, chose a partially matched (PM) MIMIC approach for the M348 power chip. The PM MIMIC consisted of a driver stage and output FET with full interstage and bias networks realized on the GaAs chip. Enough input and output matching was incorporated into the chip design to assure input and output impedances that could be easily matched within the 7-11 GHz band of interest with little or no compromise in power and efficiency performance. Using this chip as a building block, numerous module configurations covering specific sub-bands and power levels could be easily designed to satisfy a number of different actual and potential applications as described below.

The initially targeted application was the Mantech for Radar T/R Modules program, requiring a 10 watt, 8.5-10.5 GHz power part. The module carrier configuration chosen involved two pairs of M348 chips combined in quadrature using Lange couplers realized on thin film alumina substrates. Operating voltage for this part was 9 volts. Demonstration modules delivered to Westinghouse for insertion into its T/R modules performed as expected.

Near the time of the completion of the MIMIC design phase of the contract a very different application for the chip presented itself. A system prime had a need for less power (≈2 watts) but broader bandwidth (7.5-10.5 vs. 8.5-10.5 GHz) than the M348 had previously been used to produce. However, since the on-chip interstage matching network of the M348 was designed for full 7-11 GHz operation, simple modifications to the off-chip input and output matching networks and a reduction in operating voltage to 7 volts resulted in a form, fit and function replacement for the MIMIC that had been designed into the customer's system. Using the existing M348 chip, this module was designed from scratch and transferred to production in eight weeks with full production of 500 modules/week being achieved only six weeks later.

It is interesting to note that had the M348 been a conventional MIMIC fully matched on chip to 50 ohms, a completely new MIMIC design would have been required to meet this new set of requirements. Under those circumstances, the first iteration of this new MIMIC would have just been completing evaluation at about the same time the 1500th power module utilizing the existing PM MIMIC was being delivered.

The M348 chip has already been, or is being, designed into at least six different X-band applications, with bandwidth requirements from <10 to 40% and power requirements up to 10 watts. These applications include custom designs for specific program insertions as well as standard Avantek products. The flexibility of the PM MIMIC approach offers the system designer the opportunity to insert MIMICs without the usual long development cycle time. More importantly, the ability to use the same chip in many different applications will generate larger volume demands for that chip. This will in turn result in significantly lower costs for all systems that use the chip, thus satisfying one of the key goals of the MIMIC program.

6.2 Foundry Fabrication of MIMIC Chips

PERF. ORGS.:	TriQuint Semiconductor; GE
KEY PERSONNEL:	Richard Y. Koyama and Dennis A. Criss (TriQuint); David C. Denning (GE)
CONTRACT NO.:	F33615-90-C-1517
FUNDING:	$2,655,623 (includes Air Force funding)
PERIOD:	10/90-12/92
COTR:	Mark Pacer

OBJECTIVES/APPROACH: The objectives of this program are twofold: (1) develop a MIMIC chip set which can be used as a vehicle for foundry fabrication, and (2) produce this chip set in volume in the foundry environment. For this program, TriQuint Semiconductor has teamed with GE to design and produce a T/R chip set using the common leg circuit (CLC) approach for application to X-band phased array radar. The chip set consists of a phase shifter with 6 bits of phase control and switched amplifier with 6 bits of gain control. The GE team has specified and designed the CLC chip set, and TriQuint has acted as the foundry to produce the prototype, and is now in production with the chip set.

PROGRESS (Source: M. Pacer, 10/92): TriQuint's wafer fabrication capability and GaAs MESFET technology makes use of two basic processes, both offered for public use: (1) the QEDA Process, which features a 1.0 μm gate depletion-mode process, and (2) the HA Process, which features a 0.5 μm gate depletion-mode process. All wafer processing is accomplished in Class 100 clean-room facilities. A Class 10 facility houses two each of 5x and 10x I-line steppers utilized for all lithographic processing. These technological capabilities are supported on a broad foundation of reliability data collected since 1983.

The production wafers fabricated for this MIMIC Phase 3 Program are being processed as one of many "foundry" runs in the TriQuint manufacturing organization. Other than the fact that this job is larger than most single orders, these wafers receive no special handling or privileges during wafer fabrication. Production for this program is based on the start of 250 wafers (12 wafer lots). Process Control Module (PCM) testing is conducted at the regular test points. Those wafers that are PCM qualified at the end of topside processing are then passed to backside processing for thinning and vias. Of these, qualified via wafers are then passed on for die-sort testing. As part of the reporting of this program, dc/RF PCM results before and after via processing, as well as dc/RF die-sort test results, will be provided to the Air Force.

At this stage, all of the production of wafer processing is complete. The last two technical tasks that remain are the carrier-based measurements of these chips and the reliability testing of several wafers. The original design simulation of the chip set accounted for the bond wires which interconnect the two chips; therefore, GE will measure carrier-based S-parameter characteristics and compare the results to the expected performance. Both of these tasks are presently ongoing; their expected completion date is 30 November 1992.

TABULATION OF PHASE 3 PROGRAMS

The summary chart appearing on the following two pages presents a record of MIMIC Phase 3 funding through Phase 3 program completion.

TABULATION OF PHASE 3 PROGRAMS

Serv	Program Title	Start/End	Prime Contractor	Contract Number	Funding ($)					
					FY89	FY90	FY91	FY92	FY93	Total
MATERIALS AND IMPROVED GaAs GROWTH TECHNIQUES										
AF	Optical Diagnostics for Wafer Char.	7/89-12/91	AT&T	F33615-89-C-1054	179,434	201,704	184,903			566,041
N	Cost Reduction in Epi Mat'ls for MMIC App.	9/92-4/94	Bandgap	N00019-92-C-0111				231,267	607,733	839,000
N	Vertical Zone Melt Growth of GaAs	10/90-12/92	M/A-COM	N00014-91-C-2000		382,794	329,767		207,568	920,129
N	MOCVD Process Technology for MESFETs	7/89-3/91	Spire	N00019-89-C-0152	300,000	213,000	32,265			545,265
A	Enhancements for MBE Prod. of MIMICs	5/89-1/91	Varian	DAAL01-89-C-0907	662,341	576,217				1,238,558
MIMIC MODELING, COMPUTER AIDED DESIGN AND MICROWAVE HARDWARE DESCRIPTION LANGUAGE										
AF	Accurate Active Models for MMICs	6/92-12/93	Compact	F33615-92-C-1038				96,481	324,629	421,110
N	Device Models for CAD in MIMIC Mfg.	5/89-5/91	Gateway	F33615-89-C-1049	70,058	113,406	40,005			223,469
A	MIMIC Hardware Description Language	11/90-2/93	Intermetrics	DAAL01-91-C-0105			229,525	383,416		612,941
A	Statistical Design Methodology	6/92-6/94	Motorola	DAAL01-92-C-0254				236,461	260,539	497,000
A	A Physical GaAs MESFET Model	4/89-4/91	NCSU	DAAL01-89-C-0906	83,498	98,278	16,238			198,014
N	MW EM Software for Massively Par. Comps	9/92-9/94	Sonnet	N00019-92-C-0096				58,178	196,822	255,000
AF	Modeling & CAD Meth. for Layout Opt.	6/89-6/91	U of Co.	N00019-89-C-0151	225,000	451,287				676,287
ON-WAFER TESTING AND AUTOMATED TESTING TECHNIQUES										
N	MIMIC On-Wafer Chips & Module Testing	6/89-4/91	Ball	N00019-89-C-0150	385,126	172,535				557,661
A	110 GHz Wafer Probing	4/92-4/93	Cascade	DAAL01-92-C-0245				169,199	168,035	337,234
A	Optical On-Wafer MIMIC Char. Techniques	5/89-5/91	COMSAT	DAAL01-89-C-0905	391,952	296,206	71,277			759,435
AF	Automated Test of Power MIMIC Wafers	7/89-1/91	M/A-COM	F30602-89-C-0039	399,000	391,983				790,983
AF	Automated MIMIC Wafer RF Test System	4/92-3/94	S-A	F333615-92-C-1037				969,261	587,450	1,556,711
AF	Non-Contact Wafer Probing	4/89-7/90	Varian	F30602-89-C-0040	313,184	137,771				450,955

PACKAGING TECHNOLOGY

N	Mil-Qual Net-Shape Mfg Process	7/92-12/93	CPS	N00019-92-C-0106				230,301	769,622	999,923
A	Advanced Multi-Chip Ceramic Package	5/89-3/92	ITT	DAAL01-89-C-0908	413,637	320,950	31,960			766,547
A	Millimeter Wave Packaging	6/92-5/94	M-M	DAAL01-92-C-0250				306,193	479,835	786,028

ADVANCED PROCESSING

N	Focused Ion Beam for Gate Processing	7/89-4/91	TRW	N00019-89-C-0149	330,000	286,942				616,942
A	HBT Dev't for Advanced Circuits	8/92-7/94	UCSD	DAAL01-92-K-0262				93,980	28,379	122,359
AF	Low Cost Ion Implanted MMW ICs	4/92-10/93	U of IL	F33615-92-C-1039				176,829	171,281	348,110

FOUNDRY FABRICATION

AF	Foundry Fabrication of MIMIC Chips	9/90-1/93	Avantek	F33615-90-C-1518		25,000	1,225,000	1,705,154*		2,955,154
AF	Foundry Fabrication of MIMIC Chips	10/90-12/92	TriQuint	F33615-90-C-1517		25,000	1,175,000	1,455,623*		2,655,623

TOTALS	3,753,233	3,693,076	3,335,943	6,112,346	3,801,896	20,696,479

* Includes USAF funding

MIMIC PHASE 3 DIRECTORY

Government

Baidy, Edward R.	Army Research Laboratory Ft. Monmouth, NJ 07703-5601	(908) 544-4816
Borsuk, Gerald M.	Naval Research Laboratory Code 6800 4555 Overlook Ave., SW Washington, DC 20375-5000	(202) 767-3525 FAX: 767-0546
Calcatera, Mark C.	WL/ELMT Wright-Patterson AFB, OH 45433-6543	(513) 255-7679 FAX: 255-4831
Carmichael, Lorna	Army Research Laboratory Ft. Monmouth, NJ 07703-5601	(908) 532-0221 FAX: 544-4323
Chang, Wayne H.	Army Research Laboratory Ft. Monmouth, NJ 07703-5601	(908) 532-0250
Cohen, Eliot	DARPA/ESTO 3701 N Fairfax Drive Arlington, VA 22203-1714	(703) 696-2214 FAX: 696-2203
Colussi, Joseph	Naval Air Development Center Code 5022 Warminster, PA 18974	(215) 441-3785
Dietrich, Harry	Naval Research Laboratory Code 6856 4555 Overlook Ave., SW Washington, DC 20375-5000	(202) 767-1381 FAX: 767-0455
Henry, Richard	Naval Research Laboratory Code 6872 4555 Overlook Ave., SW Washington, DC 20375-5000	(202) 767-3671 FAX: 767-1165
Layden, Owen	Army Research Laboratory Ft. Monmouth, NJ 07703-5601	(908) 544-2378 FAX: 532-0722
Letellier, J.P.	Naval Research Laboratory Code 5320 4555 Overlook Ave., SW Washington, DC 20375-5000	(202) 767-2937 FAX: 767-3658

Government

May, Capt. Dennis	WL/ELM Wright-Patterson AFB, OH 45433-6543	(513) 255-7679 FAX: 255-8656
McEwen, Thomas	AF(RL)/OCTP Griffiss AFB, NY 13441-5700	(315) 330-4381 FAX: 330-2139
Novak, Mark	AF(RL)/OCTP Griffiss AFB, NY 13441-5700	(315) 330-4381 FAX: 330-2139
Pacer, Mark	WL/ELMT Wright-Patterson AFB, OH 45433-6543	(513) 255-7699 FAX 255-8656
Paolella, Arthur C.	Army Research Laboratory Ft. Monmouth, NJ 07703-5302-5601	(908) 544-2825 FAX: 544-4323
Paul, Bradley	WL/ELMT Wright-Patterson AFB, OH 45433-6543	(513) 255-7675
Quach, Tony	WL/ELMD Wright-Patterson AFB, OH 45433-6543	(513) 255-9389 FAX 255-8656
Rhodes, David	Army Research Laboratory Ft. Monmouth, NJ 07703-5601	(908) 532-0593
Ross, R. Lee	Army Research Laboratory Ft. Monmouth, NJ 07703-5601	(908) 544-2360 FAX: 544-4323
Schweller, Ron	WL/ELM Wright-Patterson AFB, OH 45433-6543	(513) 255-9391
Sleger, Kenneth J.	Naval Research Laboratory Code 6801 4555 Overlook Ave., SW Washington, DC 20375-5000	(202) 767-3894 FAX: 767-0546
Sobolewski, Elissa	DARPA/ESTO 3701 N. Fairfax Drive Arlington, VA 22203-1714	(703) 696-2254 FAX: 696-2203
Webb, Dennis C.	Naval Research Laboratory Code 6850 4555 Overlook Avenue, SW Washington, DC 20375-5000	(202) 767-3312
Worley, Rick	WL/ELMD Wright-Patterson AFB, OH 45433-6543	(513) 255-7665 FAX: 255-8656

Industry

Adams, Richard	Cermics Process Systems 155 Fortune Blvd. Milford, MA 01757	(508) 634-3422 FAX: 478-0946
Anholt, Robert E.	Gateway Modeling, Inc. 1604 East River Terrace Minneapolis, MN 55414	(612) 339-4239
Asbeck, Peter	Univ. of California, San Diego ECE Dept. LaJolla, CA 92093-0407	(619) 534-6713
Barton, David L.	Intermetrics, Inc. 7918 Jones Branch Drive Suite 710 McLean, VA 22102	(703) 827-2606 FAX: 827-5560
Berenz, John	TRW One Space Park M5/2422 Redondo Beach, CA 90278	(213) 814-1983
Brady, Vernon	Martin Marietta Corp. P.O. Box 555837 Orlando, FL 32855	(407) 356-4015
Bullock, Graham	Motorola, Inc. 8220 East Roosevelt P.O. Box 9040 Mail Drop R7211 Scottsdale, AZ 85252	(602) 441-5852 FAX: 441-5749
Caldwell, O.M.	Scientific-Atlanta Electronic Systems Division 3845 Pleasantdale Road Atlanta, GA 30340-4266	(404) 903-2141 FAX: 903-2166
Cangellaris, Prof. Andreas	University of Arizona Dept. of Electrical & Computer Engineering Tucson, AZ 85721	(602) 621-4521
Carlson, Douglas	M/A COM, Inc. Lowell Semicondutor Operations 100 Chelmsford Street Lowell, MA 01851	(508) 453-3100 Ext. 4932

Industry

Carraway, John	Martin Marietta Missile Sys. P.O. Box 555837, MP-088 Orlando, FL 32855-5837	(407) 356-4276 FAX: 356-6980
Carver, Gary	AT&T Bell Laboratories P.O. Box 900 Princeton, NJ 08540	(609) 639-2685 FAX: 639-2343
Chang, Prof. David C.	University of Colorado Center for Microwave and Millimeter-Wave Computer-Aided Design University of Colorado Campus Box 425 Boulder, CO 80309-0425	(303) 492-6702
Chauchard, E.	University of Maryland Engineering Bldg., Rm 1155C College Park, MD 20742	(301) 454-6832
Cooper, Thomas L.	Varian Associates Thin Film Div., MBE Operation 3550 Bassett Street Santa Clara, CA 95054-2704	(408) 496-2283 FAX: 727-7350
Criss, Dennis A.	TriQuint Semiconductor Inc. PO Box 4935 Beaverton, OR 97076	(503) 644-3535
Daly, Jim	Spire Corp. Patriots Park Bedford, MA 01730	(617) 275-6000 Ext. 339
Deoul, Evan	Westinghouse Electric Corp. PO Box 746 MS 75 Baltimore, MD 21203	(301) 765-2843
Eckstein, J.N.	Varian Associates 611 Hansen Way Palo Alto, CA 94303	(415) 424-5081
Ersland, Peter	M/A-COM, Inc. Advanced Semiconductor Division 100 Chelmsford Street Lowell, MA 01851	(508) 453-3100

Industry

Feng, Milton	University of Ilinois-Urbana ECE Dept.1406 W. Green Street Urbana, IL 61801	(217) 333-8080
Fullerton, Craig	Motorola, Inc. 8220 East Roosevelt P.O. Box 9040 Mail Drop R1210 Scottsdale, AZ 85252	(602) 444-4251
Godshalk, Edward	Cascade Microtech, Inc. 14255 SW Brigadoon Court Beaverton, OR 97005	(503) 626-8245 Ext. 206
Hoffman, Kenneth	ITT Defense Dept. 62001 100 Kingsland Road Clifton, NJ 07014-1993	(201) 284-2259 FAX: 284-3059
Huang, H.C.	COMSAT Laboratories Microelectronics Division 22300 Comsat Drive Clarksburg, MD 20871	(301) 428-4133 FAX: 428-7747
Jansen, Nick	M/A-COM, Inc. Advanced Semiconductor Division 100 Chelmsford Street Lowell, MA 01851	(508) 453-3100 Ext. 4875
Joseph, T.	TRW ETD/SEG One Space Park (R6-1456) Redondo Beach, CA 90278	(213) 814-1699
Kanber, Hilda	Hughes Aircraft Co. Microwave Products Divison 3100 Fujita St. P. O. Box 2940 Torrance, CA 90509	(213) 517-6408
Koos, Greg	AT&T Bell Laboratories P.O. Box 900 Princeton, NJ 08540	(609) 639-2463 FAX: 639-2343
Koyama, Richard Y.	TriQuint Semiconductor Inc. PO Box 4935 Beaverton, OR 97076	(503) 644-3535

Industry

Lanteri, Jean-Piere	M/A-COM, Inc. Advanced Semiconductor Division 100 Chelmsford Street Lowell, MA 01851	(508) 453-3100 Ext. 4945
Lee, C.H.	University of Maryland Engineering Bldg., Rm S1141 College Park, MD 20742	(301) 454-6832
Lee, T.T.	COMSAT Laboratories Microelectronics Division 22300 Comsat Drive Clarksburg, MD 20871	(301) 428-4178 FAX: 428-7747
Linden, Kurt	Spire Corp. Patriots Park Bedford, MA 01730	(617) 275-6000 Ext. 338
Luscher, P.E.	Varian Associates Thin Film Div., MBE Operation 3550 Bassett Street Santa Clara, CA 95054-2704	(408) 986-9888 Ext. 2814
Maiorino, Cesar	M/A-COM, Inc. Advanced Semiconductor Division 100 Chelmsford Street Lowell, MA 01851	(508) 453-3100 Ext. 4968
Malbon, Robert	Avantek, Inc. 3175 Bowers Ave. Santa Clara, CA 95054-3292	(408) 970-2703
Miers, Tom H.	Ball Aerospace Systems Division 10 Longs Peak Drive Broomfield, CO 80020	(303) 460-2484
Moise, Patrica	Spire Corp. Patriots Park Bedford, MA 01730	(617) 275-6000 Ext. 216
Novich, Bruce	Ceramics Process Systems 155 Fortune Blvd. Milford, MA 01757	(508) 634-3422 FAX: 478-0946
Ohlhaver, Tina	Avantek, Inc. 3175 Bowers Ave. Santa Clara, CA 95054-3292	(408) 970-2703

Industry

O'Neil, Thomas J.	Bandgap Technology 325 Interlocken Parkway Broomfield, CO 80021	(503) 460-0700 FAX: 466-0290
Perri, John	Varian Associates 611 Hansen Way Palo Alto, CA 94303	(415) 424-6989 FAX: 424-6988
Powell, Ron A.	Varian Associates Thin Film Div., MBE Operation, Bldg. 7 611 Hansen Way Palo Alto, CA 94303	(415) 424-5078 FAX: 424-6988
Rautio, James C.	Sonnet Software 135 Old Cove Road Suite 203 Liverpool, NY 13090-3746	(315) 453-3096
Riaziat, Majid	Varian Associates 611 Hansen Way Palo Alto, CA 94303	(415) 424-6277 FAX: 424-6988
Robinson, William	MicroBeam, *Inc.* 1125 Business Center Drive Newbury Park, CA 91320	(805) 499-8502
Schineller, Ronald	ITT Avionics 100 Kingland Road Clifton, NJ 07014-1993	(908) 284-2481
Stearman, Pamela	Intermetrics, Inc. 7918 Jones Branch Drive Suite 710 McLean, VA 22102	(703) 827-2606 FAX: 827-5560
Tayrani, Reza	Compact Software 483 McLean Blvd & Corner of 18th Avenue Paterson, NJ 07504	(201) 881-1200 FAX: 881-8361
Trew, Robert J.	North Carolina State University Electrical and Computer Engineering Department Box 7911 Raleigh, NC 27695-7911	(919) 737-2336 FAX: 737-3027

Industry

Tuttle, William L.	Scientific-Atlanta Electrical Sys. Division 3845 Pleasantdale Road Atlanta, GA 30340-4266	(404) 903-2141 FAX: 903-2166
Vaughn, John	GaAs Materials Manager M/A-COM, Inc. Advanced Semiconductor Division 100 Chelmsford Street Lowell, MA 01851	(508) 453-3100 Ext. 4816
Weng, S-L	Varian Associates Thin Film Division, MBE Operation 3550 Bassett Street Santa Clara, CA 95054-2704	(408) 986-9888 Ext. 2816
Zaleckas, Vincent J.	AT&T Bell Laboratories/ERC P.O. Box 900 Princeton, NJ 08540	(609) 639-2311 FAX: 639-2343